SH366301R6/008R6Y-AAA00

CONTENTS

1 General Description

SH366301 is a protection IC for lithium-ion/ lithium polymer rechargeable batteries, including voltage detection circuits with strict accuracy and delay circuits. It aims for protecting 1-cell lithium-ion/ lithium polymer rechargeable battery packs from overcharged, overdischarged, and over-current status.

The SH366301 is a high voltage tolerance CMOS-based protection IC for rechargeable one-cell lithium-ion/ lithium polymer battery,aiming to detect over-charged/over-discharged status of one-cell Li+,along with excessive load current and charge current, protect the battery from the conditions described above. What's more,SH366301 contains short-circuit protector function to prevent excessive short-circuit current.

When the SH366301 detects over-charged voltage or charging over-current, the output of CHG pin switches to "L"(low) level after the internally fixed delay time. When the SH366301 detects over-discharged voltage or discharging over-current, the output of DSG pin switches to "L"(low) level after the internally fixed delay time.

After detecting over-charged voltage, the output of CHG can returns "H"(high) when one of the two following requirements is met:

(1)the cell voltage decreases lower than V_{OVR} (over-charged release voltage);

(2)the cell voltage decreases lower than V_{OV} (over-charged detection voltage),and a discharging current is detected (the load is connected to the circuit).

After detecting over-discharged voltage, the output of DSG pin returns to "H" when one of the two following requirements is met.

(1)The cell voltage increases higher than V_{UVR} (over-discharged release voltage);

(2) the cell voltage gets higher than V_{UV} (over-discharged detection voltage),and a charger is connected.

When the charging over-current is detected,SH366301 will quit the charging over-current status and CHG returns to "H" level if the load circuit is connected.

When the discharging over-current or short-circuit current is detected, SH366301 will quit the discharging over-current or short-circuit status and DSG pin returns to "H" level if the load circuit is removed.

Part.No	V_{OV} **(V)**	V_{OVR} **(V)**	V_{UV} **(V)**	V_{UVR} **(V)**	V_{DOC1} **(mV)**	V_{DOC2} **(mV)**	V_{SC} **(mV)**	V_{SC2} **(YES/NO)**	V_{COC} **(mV)**
SH366301R6/008R6Y-AAA00	4.475	4.325	2.350	2.550	10.5	15	40	YES	-15

续上表：

Part.No	t_{OV} **(s)**	t_{UV} **(ms)**	t_{DOC1} **(s)**	t_{DOC2} **(ms)**	t_{SC} **(μs)**	t_{COC} **(ms)**	t_{CTL} **(ms)**	0V battery Charge **(Allowed/ Forbidden)**	Power Down Mode **(YES/NO)**
SH366301R6/008R6Y-AAA00	1.0	64	3.584	16	280	16	48	Allowed	YES

2 Block Diagram

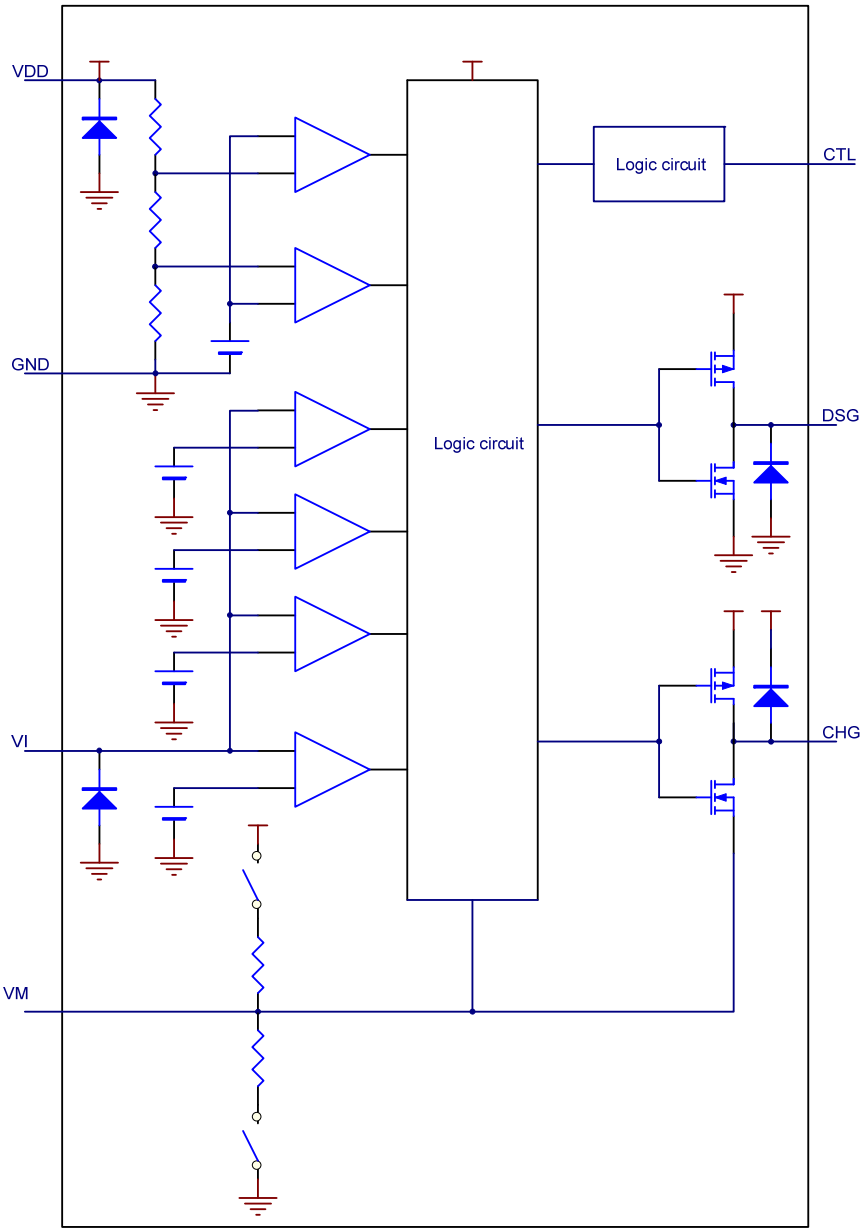


Fig 1. SH366301 Block Diagram

3 Pin Descriptions

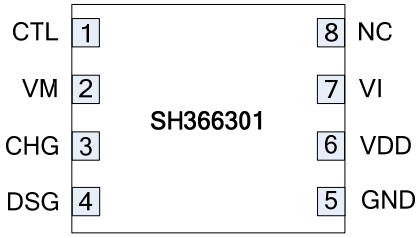


Fig 2. Pin Configuration of SH366301

Table1. SH366301 pin description (Total 8 pins.)

Pin NO.	Pin Name	I/O	Function Description
1	CTL	I	Input pin to control charge or discharge
2	VM	I	Load and charger detection pin;
3	CHG	O	Drive pin of charge MOSFET;
4	DSG	O	Drive pin of discharge MOSFET;
5	GND	I	Input pin for negative power supply;
6	VDD	I	Input pin for positive power supply;
7	VI	I	Current detection pin;
8	NC	-	No connection ;

4 Absolute maximum ratings

(Ta=25°C,GND=0V)

Item	Pin Name	Absolute maximum ratings	Unit
Input voltage between VDD pin and GND pin	VDD	GND-0.3 to GND+6.0	V
VI/CTL input voltage	VI/CTL	GND-0.3 to VDD+0.3	V
VM pin input voltage	VM	VDD-28 to VDD+0.3	V
CHG pin output voltage	CHG	V_{VM}-0.3 to VDD+0.3	V
DSG pin output voltage	DSG	GND-0.3 to VDD+0.3	V
Operation ambient temperature	-	-40 to 85	°C
Storage temperature	-	-55 to 125	°C

Note1： ***If the actual operating parameter exceeds the range of absolute maximum ratings,the components of SH366301 will be permanently damaged. Only when the operating parameters are among the regulated range above, the relevant functions can be guaranteed in normal working status.***

5 Electrical characteristics

5.1 Electrical characteristics(unless otherwise specified, Ta=25°C)

Symbol	Item	Min.	Typ.	Max.	Unit	Test Circuit
V_{OV}	Overcharge detection voltage	4.455	4.475	4.495	V	A
V_{OVR}	Overcharge release voltage	4.275	4.325	4.375	V	A
t_{OV}	Overcharge detection delay time	0.7	1.0	1.3	s	B
t_{OVR}	Overcharge release delay time	0.65	1.0	1.5	ms	B
t_{OVHR}	Overcharge hysteresis release delay time	160	250	375	μs	B
V_{UV}	Overdischarge detection voltage	2.300	2.350	2.400	V	A
V_{UVR}	Overdischarge release voltage	2.475	2.550	2.625	V	A
t_{UV}	Overdischarge detection delay time	44.8	64.0	83.2	ms	B
t_{UVR}	Overdischarge release delay time	0.7	5.0	11.7	ms	B
t_{UVHR}	Overdischarge hysteresis release delay time	0.65	1.0	1.5	ms	B
t_{PD}	delay time of entering Power Down Mode	0.4	1.0	2.5	ms	B
t_{PDR}	delay time of quitting Power Down Mode	0.7	1.0	1.3	ms	B
V_{DOC1}	Discharge overcurrent 1 detection voltage	9.0	10.5	12.0	mV	B
t_{DOC1}	Discharge overcurrent 1 detection delay time	2.509	3.584	4.659	s	B
V_{DOC2}	Discharge overcurrent 2 detection voltage	12	15	18	mV	B
t_{DOC2}	Discharge overcurrent 2 detection delay time	11.2	16.0	20.8	ms	B
V_{SC}	Short circuit detection voltage	36	40	44	mV	B
t_{SC}	Short circuit detection delay time	196	280	364	μs	B
V_{SC2}	Short circuit 2 detection voltage	VDD-1.4	VDD-0.8	VDD-0.3	V	B
V_{DOCR}	Discharge overcurrent release voltage	0.78*VDD	0.83*VDD	0.86*VDD	V	B
t_{DOCR}	Discharge overcurrent release delay time	0.65	1.0	1.5	ms	B
V_{COC}	Charge overcurrent detection voltage	-16.5	-15.0	-13.5	mV	B
t_{COC}	Charge overcurrent detection delay time	11.2	16.0	20.8	ms	B
t_{COCR}	Charge overcurrent release delay time	160	250	375	μs	B

Symbol	Item	Min.	Typ.	Max.	Unit	Test Circuit
V_{CHGH}	CHG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{DSGH}	DSG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{LD}	Load detection voltage	0.3	0.35	0.4	V	B
V_{CD1}	Charger detection voltage	GND-0.01	GND	GND+0.01	V	B
V_{CD2}	Charger detection voltage 2	0.6	0.7	1.2	V	B
V_{CTL}	CTL voltage	0.6	0.8	1.2	V	B
V_{0CHA}	Minimum charger voltage	0.7	1.1	1.5	V	D
I_{CC}	Operating current (normal mode)	1	2	3	μA	C
I_{PD}	Current consumption of sleep status	0.01	0.03	0.05	μA	C
R_{DH}	Internal pull-up resistance of DSG pin	0.5	1.0	1.7	kΩ	D
R_{CH}	Internal pull-up resistance of CHG pin	1.2	2.5	5.0	kΩ	D
R_{DL}	Internal pull-down resistance of DSG pin	2.1	3.1	4.1	kΩ	D
R_{CL}	Internal pull-down resistance of CHG pin	1.6	2.5	4.0	kΩ	D
t_{DH}	The time during the period that the DSG pin rises from GND to VDD-0.5	3	8	15	μs	E
t_{DL}	The time during the period that the DSG pin decreases from VDD-0.5 to GND	10	35	100	μs	E
t_{CH}	The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5	10	25	40	μs	E
t_{CL}	The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM	15	47	60	μs	E
t_{CTL}	delay time of inhibition for charging and discharging	33.6	48.0	62.4	ms	B
t_{CTLR}	delay time of inhibition release for charging and discharging	11.2	16.0	20.8	ms	B
R_{VMS}	Internal pull-down resistance of VM pin	7.5	10	15	kΩ	D
R_{VMD}	Internal pull-up resistance of VM pin	0.5	1.25	2.5	MΩ	D
R_{CTL}	Internal resistance of CTL pin	2.50	5.00	10.00	MΩ	C

5.2 Electrical characteristics(unless otherwise specified, Ta=-25°C~70°C)

Symbol	Item	Min.	Typ.	Max.	Unit	Test Circuit
V_{OV}	Overcharge detection voltage	4.450	4.475	4.500	V	A
V_{OVR}	Overcharge release voltage	4.270	4.325	4.380	V	A
t_{OV}	Overcharge detection delay time	0.6	1.0	1.4	s	B
t_{OVR}	Overcharge release delay time	0.5	1.0	2.0	ms	B
t_{OVHR}	Overcharge hysteresis release delay time	125	250	500	μs	B
V_{UV}	Overdischarge detection voltage	2.295	2.350	2.405	V	A
V_{UVR}	Overdischarge release voltage	2.465	2.550	2.635	V	A
t_{UV}	Overdischarge detection delay time	38.4	64.0	89.6	ms	B
t_{UVR}	Overdischarge release delay time	0.6	5.0	12.6	ms	B
t_{UVHR}	Overdischarge hysteresis release delay time	0.5	1.0	2.0	ms	B
t_{PD}	delay time of entering Power Down Mode	0.4	1.0	2.5	ms	B
t_{PDR}	delay time of quitting Power Down Mode	0.6	1.0	1.4	ms	B
V_{DOC1}	Discharge overcurrent 1 detection voltage	8.5	10.5	12.5	mV	B
t_{DOC1}	Discharge overcurrent 1 detection delay time	2.330	3.584	4.838	s	B
V_{DOC2}	Discharge overcurrent 2 detection voltage	12	15	18	mV	B
t_{DOC2}	Discharge overcurrent 2 detection delay time	9.6	16	22.4	ms	B
V_{SC}	Short circuit detection voltage	35.5	40.0	44.5	mV	B
t_{SC}	Short circuit detection delay time	168	280	392	μs	B
V_{SC2}	Short circuit 2 detection voltage	VDD-1.4	VDD-0.8	VDD-0.3	V	B
V_{DOCR}	Discharge overcurrent release voltage	0.78*VDD	0.83*VDD	0.86*VDD	V	B
t_{DOCR}	Discharge overcurrent release delay time	0.5	1.0	2.0	ms	B
V_{COC}	Charge overcurrent detection voltage	-17	-15	-13	mV	B
t_{COC}	Charge overcurrent detection delay time	9.6	16.0	22.4	ms	B
t_{COCR}	Charge overcurrent release delay time	125	250	500	μs	B

Symbol	Item	Min.	Typ.	Max.	Unit	Test Circuit
V_{CHGH}	CHG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{DSGH}	DSG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{LD}	Load detection voltage	0.3	0.35	0.4	V	B
V_{CD1}	Charger detection voltage	GND-0.01	GND	GND+0.01	V	B
V_{CD2}	Charger detection voltage 2	0.6	0.7	1.2	V	B
V_{CTL}	CTL voltage	0.6	0.8	1.2	V	B
V_{0CHA}	Minimum charger voltage	0.5	1.1	1.7	V	D
I_{CC}	Operating current (normal mode)	1	2	4	μA	C
I_{PD}	Current consumption of sleep status	0.01	0.03	0.10	μA	C
R_{DH}	Internal pull-up resistance of DSG pin	0.5	1.0	1.7	kΩ	D
R_{CH}	Internal pull-up resistance of CHG pin	1.2	2.5	5.0	kΩ	D
R_{DL}	Internal pull-down resistance of DSG pin	2.1	3.1	4.1	kΩ	D
R_{CL}	Internal pull-down resistance of CHG pin	1.6	2.5	4.0	kΩ	D
t_{DH}	The time during the period that the DSG pin rises from GND to VDD-0.5	3	8	15	μs	E
t_{DL}	The time during the period that the DSG pin decreases from VDD-0.5 to GND	10	35	100	μs	E
t_{CH}	The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5	10	25	40	μs	E
t_{CL}	The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM	15	47	60	μs	E
t_{CTL}	delay time of inhibition for charging and discharging	28.8	48.0	67.2	ms	B
t_{CTLR}	delay time of inhibition release for charging and discharging	9.6	16.0	22.4	ms	B
R_{VMS}	Internal pull-down resistance of VM pin	7.5	10	15	kΩ	D
R_{VMD}	Internal pull-up resistance of VM pin	0.25	1.25	3.50	MΩ	D
R_{CTL}	Internal resistance of CTL pin	1.25	5.00	15.00	MΩ	C

5.3 Electrical characteristics(unless otherwise specified, Ta=-40°C~85°C)

Symbol	Item	Min.	Typ.	Max.	Unit	Test Circuit
V_{OV}	Overcharge detection voltage	4.440	4.475	4.510	V	A
V_{OVR}	Overcharge release voltage	4.265	4.325	4.385	V	A
t_{OV}	Overcharge detection delay time	0.5	1.0	1.5	s	B
t_{OVR}	Overcharge release delay time	0.5	1.0	2.0	ms	B
t_{OVHR}	Overcharge hysteresis release delay time	150	250	500	μs	B
V_{UV}	Overdischarge detection voltage	2.290	2.350	2.410	V	A
V_{UVR}	Overdischarge release voltage	2.450	2.550	2.650	V	A
t_{UV}	Overdischarge detection delay time	32	64	96	ms	B
t_{UVR}	Overdischarge release delay time	0.5	5.0	13.5	ms	B
t_{UVHR}	Overdischarge hysteresis release delay time	0.5	1.0	2.0	ms	B
t_{PD}	delay time of entering Power Down Mode	0.4	1.0	2.5	ms	B
t_{PDR}	delay time of quitting Power Down Mode	0.5	1.0	1.5	ms	B
V_{DOC1}	Discharge overcurrent 1 detection voltage	8.5	10.5	12.5	mV	B
t_{DOC1}	Discharge overcurrent 1 detection delay time	1.792	3.584	5.376	s	B
V_{DOC2}	Discharge overcurrent 2 detection voltage	11.5	15.0	18.5	mV	B
t_{DOC2}	Discharge overcurrent 2 detection delay time	8	16	24	ms	B
V_{SC}	Short circuit detection voltage	35.5	40.0	44.5	mV	B
t_{SC}	Short circuit detection delay time	140	280	420	μs	B
V_{SC2}	Short circuit 2 detection voltage	VDD-1.4	VDD-0.8	VDD-0.3	V	B
V_{DOCR}	Discharge overcurrent release voltage	0.78*VDD	0.83*VDD	0.86*VDD	mV	B
t_{DOCR}	Discharge overcurrent release delay time	0.5	1.0	2.0	ms	B
V_{COC}	Charge overcurrent detection voltage	-17	-15	-13	mV	B
t_{COC}	Charge overcurrent detection delay time	8	16	24	ms	B
t_{COCR}	Charge overcurrent release delay time	125	250	500	μs	B

Symbol	Item	Min.	Typ.	Max.	Unit	Test Circuit
V_{CHGH}	CHG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{DSGH}	DSG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{LD}	Load detection voltage	0.30	0.35	0.40	V	B
V_{CD1}	Charger detection voltage	GND-0.01	GND	GND+0.01	V	B
V_{CD2}	Charger detection voltage 2	0.6	0.7	1.2	V	B
V_{CTL}	CTL voltage	0.6	0.8	1.2	V	B
V_{0CHA}	Minimum charger voltage	0.5	1.1	1.7	V	D
I_{CC}	Operating current (normal mode)	1	2	4	μA	C
I_{PD}	Current consumption of sleep status	0.01	0.03	0.10	μA	C
R_{DH}	Internal pull-up resistance of DSG pin	0.5	1.0	1.7	kΩ	D
R_{CH}	Internal pull-up resistance of CHG pin	1.2	2.5	5.0	kΩ	D
R_{DL}	Internal pull-down resistance of DSG pin	2.1	3.1	4.1	kΩ	D
R_{CL}	Internal pull-down resistance of CHG pin	1.6	2.5	4.0	kΩ	D
t_{DH}	The time during the period that the DSG pin rises from GND to VDD-0.5	3	8	15	μs	E
t_{DL}	The time during the period that the DSG pin decreases from VDD-0.5 to GND	10	35	100	μs	E
t_{CH}	The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5	10	25	40	μs	E
t_{CL}	The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM	15	47	60	μs	E
t_{CTL}	delay time of inhibition for charging and discharging	24	48	72	ms	B
t_{CTLR}	delay time of inhibition release for charging and discharging	8	16	24	ms	B
R_{VMS}	Internal pull-down resistance of VM pin	7.5	10	15	kΩ	D
R_{VMD}	Internal pull-up resistance of VM pin	0.25	1.25	3.5	MΩ	D
R_{CTL}	Internal resistance of CTL pin	1.25	5.00	15.00	MΩ	C

Note2： ***The current flowing into the chip is negative, such as leak current. The current flowing out of the chip is positive, such as power consumption, pull current.***

Note3： ***Refer to test circuits in chapter 7.***

6 Function Description

6.1 Normal status

When all the following conditions are satisfied, SH366301 is in normal status:

(1). The battery voltage is between V_{UV}(over-discharged detection voltage) and V_{OV}(over-charged detection voltage);

(2). The VI pin voltage of SH366301 is between V_{COC}(charging over-current detection voltage) and V_{DOC1} (discharging over-current 1 detection voltage);

(3). CHG pin outputs VDD, DSG pin outputs VDD,charge and discharge MOSFET are both turned on.

6.2 Over-charged status

When all the following conditions are satisfied, SH366301 enters over-charged status and turns off the charge MOSFET:

(1). The battery voltage is higher than V_{OV} (over-charged detection voltage);

(2). The condition of (1) lasts up to t_{OV} (over-charged detection delay time) or longer;

When one of the following conditions is satisfied, the over-charged status is released, and the charge MOSFET is turned on:

(1). The voltage of the VM pin is lower than V_{LD}(without load connection), and the cell voltage is lower than V_{OVR} (over-charged release voltage),lasting up to t_{OVR} (over-charged release delay time) or longer;

(2). The voltage of the VM pin is higher than V_{LD} (with load connection), lasting up to t_{OVHR} (over-charged release hysteresis delay time) or longer, and the cell voltage is lower than V_{OV} (over-charged detection voltage);

Note4： When SH366301 is in overcharge status,the discharging over-current detection and short-circuit detection function is disabled .

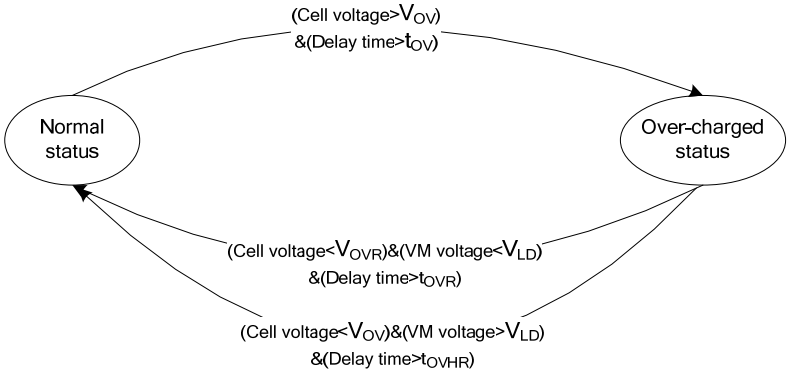


Fig 3. Over-charged Protection

6.3 Over-discharged status

When all the following conditions are satisfied, SH366301 enters over-discharged status and turns off the discharge MOSFET,the internal pull-up resistance is also turned on:

(1). The cell voltage is lower than V_{UV}(over-discharged detection voltage);

(2). The condition (1) lasts up to t_{UV} (over-discharged detection delay time) or longer;

When one of the following conditions is satisfied, the over-discharged status is released, and the discharge MOSFET is turned on:

(1). The voltage of the VM pin is not lower than V_{CD1} (without charger plugged in), and the cell voltage is higher than V_{UVR} ,lasting up to t_{UVR}(delay time of over-discharged release detection);

(2). The voltage of the VM pin is lower than V_{CD1} (with charger plugged in),lasting up to t_{UVHR} (delay time of over-discharged release hysteresis) or longer, and the cell voltage is higher than V_{UV}(over-discharged detection voltage);

Note5： When cell voltage is lower than V_{UV},the charging overcurrent detection function is disabled.

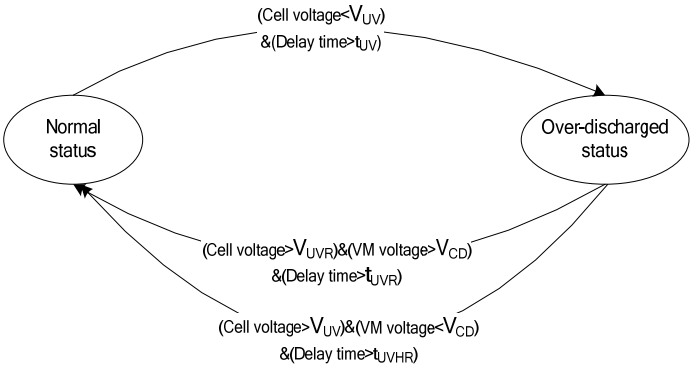


Fig 4. Over-discharged Protection

6.4 Power Down status

When the system is over-discharged,SH366301 will enter Power Down status when all the following conditions are satisfied,and the internal pull-up resistance of SH366301 is turned on:

(1).The voltage of VM pin is higher than VDD-0.8;

(2). The condition of (1) lasts for longer thatt_{PD} (delay time of entering power down status).

When system is in Power Downstatus,SH366301 will quit the Power Downstatus when all the following conditions are satisfied,and the system enters into over-discharged status.

(1).The voltage of VM pin is lower than V_{CD2}(typical value of charger detection voltage2);

(2).The condition of (1) lasts for longer than t_{PDR} (delay time of quitting power down state).

6.5 Discharging over-current status

SH366301 has three levels for discharging over-current protection, V_{DOC1} (discharging over-current 1 detection voltage) is lower than V_{DOC2} (discharging over-current 2 detection voltage)， V_{DOC2} is lower than V_{SC}(short-circuit detection voltage), t_{DOC1} (delay time of discharging over-current detection 1) is larger than t_{DOC2} (delay time of discharging over-current 2 detection), t_{DOC2} is larger than t_{SC} (short-circuit detection delay time).

When all the following conditions are satisfied, SH366301 enters discharging over-current status and turns off the discharge MOSFET:

(1). The VI pin voltage of SH366301 is higher than V_{DOC1}/V_{DOC2}/ V_{SC};

(2). The condition (1) lasts up to t_{DOC1}/t_{DOC2}/t_{SC};

When all the following conditions are satisfied, the discharging over-current status is released:

(1). Load is removed or charger is connected(the VM voltage is lower than V_{DOCR});

(2). The condition (1) lasts up to t_{DOCR} (delay time of discharging over-current release).

Note6： When SH366301 is in discharging over-current status, SH366301 will turn on the internal pull-down resistance and pull VM pin down to GND,in order to judge whether the outside load is removed.

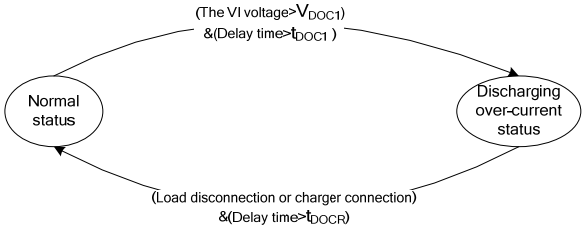


Fig 5. Discharging over-current 1 Protection

6.6 Discharging short-circuit 2 status

SH366301 contains discharging short-circuit 2 protection,when both of the following conditions are satisfied,system enters discharging short-circuit 2 status and turns off the discharge MOSFET:

(1). The VM pin voltage is higher than V_{SC2}(discharging short-circuit 2 detection voltage);

(2). The condition (1) lasts up to t_{SC};

When all the following conditions are satisfied, the discharging short-circuit 2 status is released:

(1). The load is disconnected or the charger is connected(the voltage of VM pin is lower than V_{DOCR});

(2). The condition (1) lasts up to t_{DOCR};

6.7 Charging over-current status

SH366301 contains charging over-current protection funtion, when all the following conditions are satisfied, system enters charging over-current status and turns off the charge MOSFET:

(1). The VI pin voltage of SH366301 is lower than V_{COC}(charging over-current detection voltage);

(2). The condition (1) lasts longer than t_{COC}(delay time of charging over-current detection);

When all the following conditions are satisfied, the charging over-current status is released:

(1). The load is connected (the voltage of the VM pin is higher than V_{LD});

(2). The condition (1) lasts longer than t_{COCR}(delay time of charging over-current release);

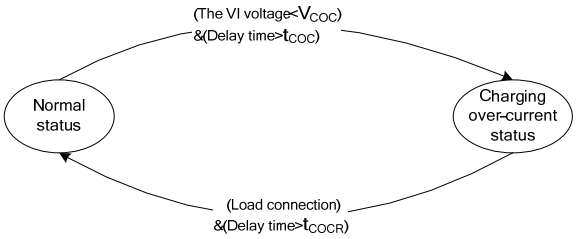


Fig 6. Charging over-current Protection

6.8 Function for 0V battery charging

When the battery voltage is 0V,the battery can be charged if using a charger the voltage of which is higher than $V_{0CHA,}$ actual required voltage of the charger varies according to the different threshold voltage of charge MOSFET.

6.9 Control logic of CTL pin

SH366301 concentrates external pin to control charge and discharge MOS, it enters charge-and-discharge inhibition status when the following conditions are satisfied :

(1).The voltage of CTL pin is higher than V_{CTL}; when voltage of CTL is in this range, we define CTL pin as in the activated condition.

(2).The condition (1) lasts longer than t_{CTL}(delay time of inhibition for charging and discharging);

When the following conditions are satisfied, the inhibition for charging and discharging will be released :

(1). The voltage of CTL pin is converted lower than V_{CTL}; when voltage of CTL is in this range, we define CTL pin as in the inactivated condition.

(2). The condition (1) lasts longer than t_{CTLR}(delay time of inhibition release for charging and discharging);

Note7： ***When the system is in over-discharged status ,the function to control charge /discharge MOS via CTL pin is disabled .***

7 Test Circuits

7-1. Overcharge detection voltage (V_{OV}) & Overcharge release voltage(V_{OVR})

【Test Circuit】: A

【Description】: Set V1=3.4V,V2 = 0V,connect VI and CTL pin to GND.Increase V1 until the voltage of CHG pin drop to low,the present V1 is V_{OV}.Then decrease V1 from present voltage,until the voltage of CHG pin returns to normal,similarly,is V_{OVR} .

7-2. Overdischarge detection voltage (V_{UV}) & Overdischarge release voltage (V_{UVR})

【Test Circuit】: A

【Description】: Set V1=3.4V,V2 = 0.1V,connect VI and CTL pin to GND.Decrease V1 until the voltage of DSG pin drop to low, the present V1 is V_{UV} .Then Increase V1 from present voltage,until DSG pin returns to normal,similarly,is V_{UVR} .

7-3. Discharge overcurrent 1 detection voltage (V_{DOC1})

【Test Circuit】: B

【Description】: Set V1=VDD-1=3.4V,V5=0V,disconnect VM from V2,connect switch 2 and switch 3,disconnect switch 1.Increase V5 until the following two requirements are satisfied.Then,the present V5 is V_{DOC1}.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V5 and shutting down of DSG is around 3.584s.

7-4. Discharge overcurrent 2 detection voltage (V_{DOC2})

【Test Circuit】: B

【Description】: Set V1=VDD-1=3.4V,V5=0V,disconnect VM from V2,connect switch 2 and switch 3,disconnect switch 1.Increase V5 until the following two requirements are satisfied.Then,the present V5 is V_{DOC2}.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V5 and shutting down of DSG is around 16ms.

7-5. Short circuit detection voltage(V_{SC})

【Test Circuit】: B

【Description】: Set V1=VDD-1=3.4V,V5=0V,disconnect VM from V2,connect switch 2 and switch 3,disconnect switch 1.Increase V5 until the following two requirements are satisfied.Then,the present V5 is V_{SC}.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V5 and shutting down of DSG is around 280μs.

7-6. Short circuit detection voltage(V_{SC2})/ Discharge overcurrent release voltage (V_{DOCR})

【Test Circuit】: C

【Description】: Set V1=VDD-1=3.4V,V2=V5=0V,connect switch 2,disconnect switch 1.Increase V2 until DSG pin shuts down,the present V2 is V_{SC2}.Then decrease V2 to 0V,decrease VDD-1 of the extra test circuit until DSG pin returns high,similarly,is $V_{DOCR.}$

7-7. Charge overcurrent detection voltage (V_{COC})

【Test Circuit】: B

【Description】: Set V1=3.4V,V2=V5=0V,connect switch 2,disconnect switch 1 and switch 3.Decrease V5 untill CHG pin shuts down.Then,the present V5 is V_{COC}.

7-8. Load detection voltage (V_{LD})

【Test Circuit】: B

【Description】: Set V1=4.7V,V2=V5=0V,connect switch 2,disconnect switch 1 and switch 3,the CHG pin turns low,then decrease V1 to 4.45V .Increase V2 till the point where CHG returns high.The present V2 is V_{LD}.

7-9．Charger detection voltage 1(V_{CD1})

【Test Circuit】：B

【Description】：Set V1=2.2V,V5=0V,V2=0.1V,connect switch 2,disconnect switch 1 and switch 3,the DSG pin turns low.Then increase V1=2.45V.Decrease V2 gradually,if V2 is decreased to 0V while DSG still keeps low,then continue decrease V2 to negative(adjustment step is 1mV),till the DSG returns high.The present V2 is the V_{CD1}.

7-10．Charger detection voltage 2(V_{CD2})

【Test Circuit】：B

【Description】：Set V1=2.2V,V5=0V,V2=1.0V,connect switch 2,disconnect switch 1 and switch 3,the DSG pin turns low.Then increase V1=2.7V.Decrease V2 gradually till the DSG returns high.The present V2 is the V_{CD2}.

7-11．CTL voltage (V_{CTL})

【Test Circuit】：B

【Description】：Set V1=3.4V,V2=V5=0V,V6=2V,connect switch1,disconnect switch 2 and switch 3,increase V6 till the point where DSG and CHG pin turn down.The present V6 is V_{CTL} (around 0.8V).

7-12．Operating current in normal mode(I_{CC})

【Test Circuit】：C

【Description】：Set V1=3.4V,V5=V2=0V, remove the extra test circuit of DSG,Connect switch 2 while disconnect switch 1,record the current at IC's VDD pin.

7-13．Current consumption of over-discharged status (I_{PD})

【Test Circuit】：C

【Description】：Set V1 =1.8V, V5=0V, disconnect V2, remove the extra test circuit of DSG,Connect switch 2 while disconnect switch 1,DSG pin turns down.Record the current at IC's VDD pin,which is $I_{PD.}$

7-14．Internal pull-down resistance of VM pin (R_{VMS})

【Test Circuit】：D

【Description】：Set V1=V2=3.4V,V5=0V,remove V3 and V4,connect switch 2 while disconnect switch 1, disconnect VM from V2,DSG pin turns low.Record the current at IC's VM pin I_{VM},then calculate the result: R_{VMS}=3.4V/I_{VM}.

7-15．Internal pull-up resistance of VM pin (R_{VMD})

【Test Circuit】：D

【Description】：Set V1=2.2V, V2=V5=0V,remove V3 and V4,connect switch 2 while disconnect switch 1.Record the current at IC's VM pin I_{VM},and calculate the R_{VMD}=V1/I_{VM}.

7-16．Internal resistance of CTL pin (R_{CTL})

【Test Circuit】：C

【Description】：Set V1=3.4V, V2=V5=0V,V6=1.0V,connect switch 2 while disconnect switch 1,system operates on normal status.Record the current at IC's CTL pin I_{CTL}.Calculate R_{CTL}=V6/ I_{CTL}.

7-17．Internal pull-up resistance of DSG pin (R_{DH})

【Test Circuit】：D

【Description】：Set V1=4.0V,V2=V5=0V,V3=V4=3.5V,connect switch 2 while disconnect switch 1,obtain the current flowing out the DSG pin I_{DO}.R_{DH}=0.5V/ $I_{DO.}$

7-18. Internal pull-up resistance of CHG pin (R_{CH})

【Test Circuit】: D

【Description】: Set V1=4.0V,V2=V5=0V,V3=V4=3.5V,connect switch 2 while disconnect switch1,obtain the current flowing out the CHG pin I_{CO}. R_{CH}=0.5V/ I_{CO}.

7-19. Internal pull-down resistance of DSG pin (R_{DL})

【Test Circuit】: D

【Description】: Set VDD=2.2V,V2=V5=0V,V4=0.1V,connect switch 2 while disconnect switch 1,system enter over-discharge protection system and DSG pin turns down.Obtain the current sinking into the DSG pin I_{CO}.R_{DL}=0.1V/ I_{CO}.

7-20. Internal pull-down resistance of CHG pin (R_{CL})

【Test Circuit】: D

【Description】: Set VDD=4.7V,V2=V5=0V,V3=0.1V,connect switch 2 while disconnect switch 1,system enter over-charge protection system and CHG pin turns down.Obtain the current sinking into the CHG pin I_{CO}.R_{DL}=0.1V/ I_{CO}.

7-21. Overcharge detection delay time (t_{OV})

【Test Circuit】: B

【Description】: Set V1=3.4V, V2=V5=0V,connect switch 2 while disconnect switch1,disconnect switch 3,system operates in normal status.Then change V1 swiftly to 4.7V,the delay time between the point where V1 is higher than the actual V_{OV} and shutting down of CHG is exactly the t_{OV}.

7-22. Overdischarge detection delay time (t_{UV})

【Test Circuit】: B

【Description】: Set V1=3.4V, V2=V5=0V,connect switch 2 while disconnect switch 1,disconnect switch 3,system operates in normal status.Then change V1 swiftly to 2.2V,the delay time between the point where V1 is lower than the actual V_{UV} and shutting down of DSG is exactly the t_{UV}.

7-23. Discharge overcurrent 1 detection delay time (t_{DOC1})

【Test Circuit】: B

【Description】: Set V1=VDD-1=3.4V,disconnect VM from V2,connect switch 2 and switch 3,disconnect switch1.Set V5=12mV,connect VI to V5 swiftly,the delay time between the rise of VI and shutting down of DSG is exactly the t_{DOC1}.

7-24. Discharge overcurrent 2 detection delay time (t_{DOC2})

【Test Circuit】: B

【Description】: Set VDD=VDD-1=3.4V, disconnect VM from V2,connect switch 2 and switch 3,disconnect switch1.Set V5=18mV,connect VI to V5 swiftly,the delay time between the rise of VI and shutting down of DSG is exactly the t_{DOC2}.

7-25. Short circuit detection voltage (t_{SC})

【Test Circuit】: B

【Description】: Set VDD=VDD-1=3.4V, disconnect VM from V2,connect switch 2 and switch 3,disconnect switch1.Set V5=45mV,connect VI to V5 swiftly,the delay time between the rise of VI and shutting down of DSG is exactly the t_{SC}.

7-26. Charge overcurrent detection delay time (t_{COC})

【Test Circuit】: B

【Description】: Set VDD=3.4V,V2=0V,connect switch 2 ,disconnect switch 3 and switch 1.Set V5=-18mV,connect VI to V5 swiftly,the delay time between the drop of VI and shutting down of CHG is exactly the t_{COC}.

7-27．delay time of inhibition for charging and discharging (t_{CTL})

【Test Circuit】：B

【Description】：Set VDD 3.4V,V2=0V, V5=0V,connect switch 1,disconnect switch 2 and switch 3,system operates in normal status.Set V6=3.4V,connect CTL to V6 swiftly.The delay time between the rise of CTL pin and the shutting down of both CHG and DSG pin is $t_{CTL.}$

7-28．delay time of inhibition release for charging and discharging (t_{CTLR})

【Test Circuit】：B

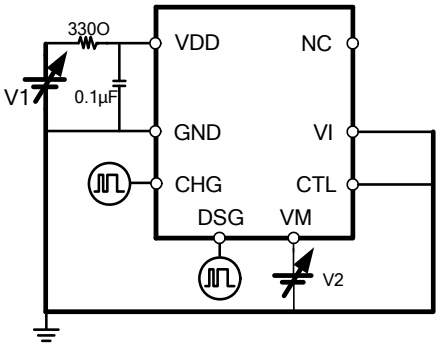
【Description】：Set VDD 3.4V,V2=0V, V6=3.4V,V5=0V,connect switch 1,disconnect switch 2 and switch 3,CHG and DSG pin turn down.Disconnect switch 3 swiftly.The delay time between the drop of CTL pin and the rise of both CHG and DSG pin is $t_{CTLR.}$

7-29．Minimum charger voltage (V_{0CHA})

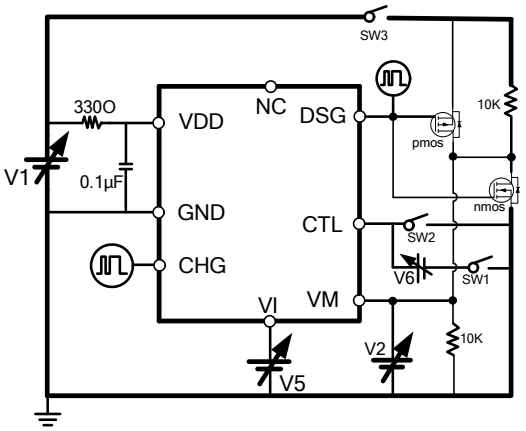
【Test Circuit】：D

【Description】：Set V1=V5=0V,V2=V3=-0.5V,connect switch 2,disconnect switch 1.Decrease V2 till the point where the current at IC's CHG pin is higher than 1.0μA.Then,the V_{0CHA}=-V2 .

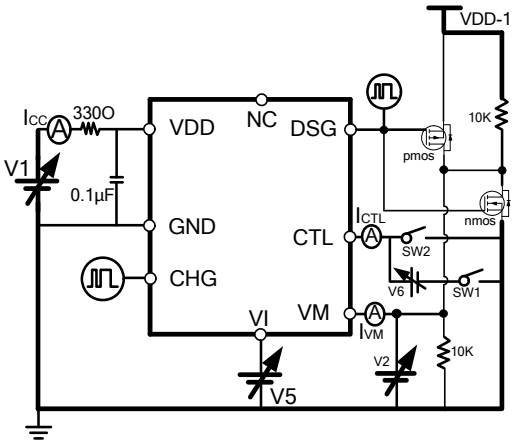
Note8： ***When testing 7-3(V_{DOC1}),7-4(V_{DOC2}),7-5(V_{SC}),7-6(V_{SC2}&V_{DOCR}),7-23(t_{DOC1}),7-24(t_{DOC2}),7-25(t_{SC}),the VDD-1 will be adjusted only in 7-6,so we should add another 3.4V to VDD-1,in the other items,the VDD-1 can be connected to V1 directly for convenience.***



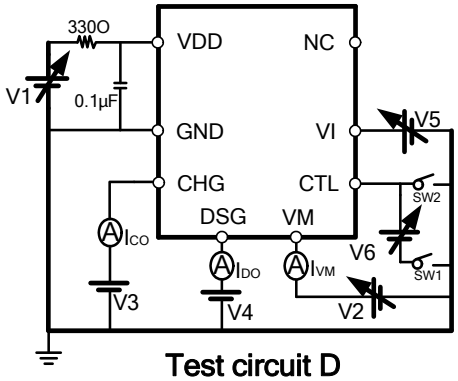
Test circuit A



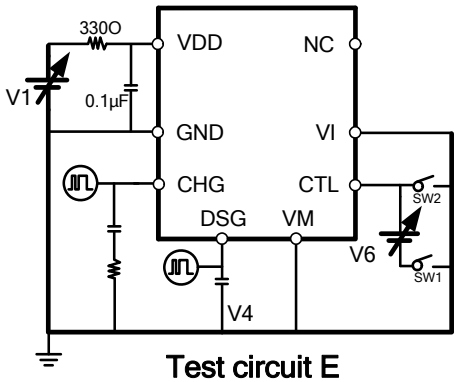
Test circuit B



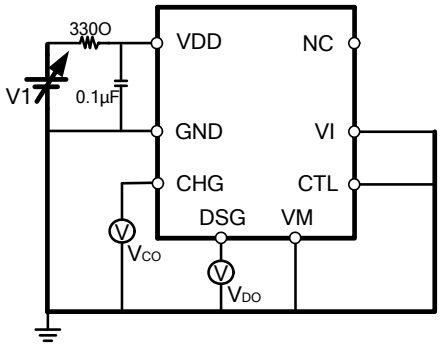
Test circuit C



Test circuit D



Test circuit E



Test circuit F

8 Typical application schematic

8.1 Application schematic of SH366301

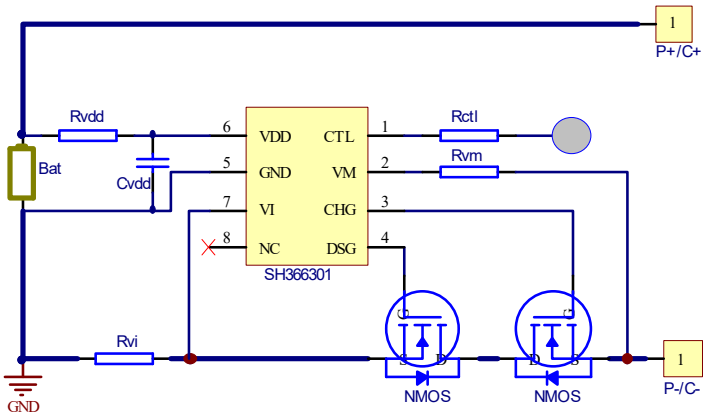


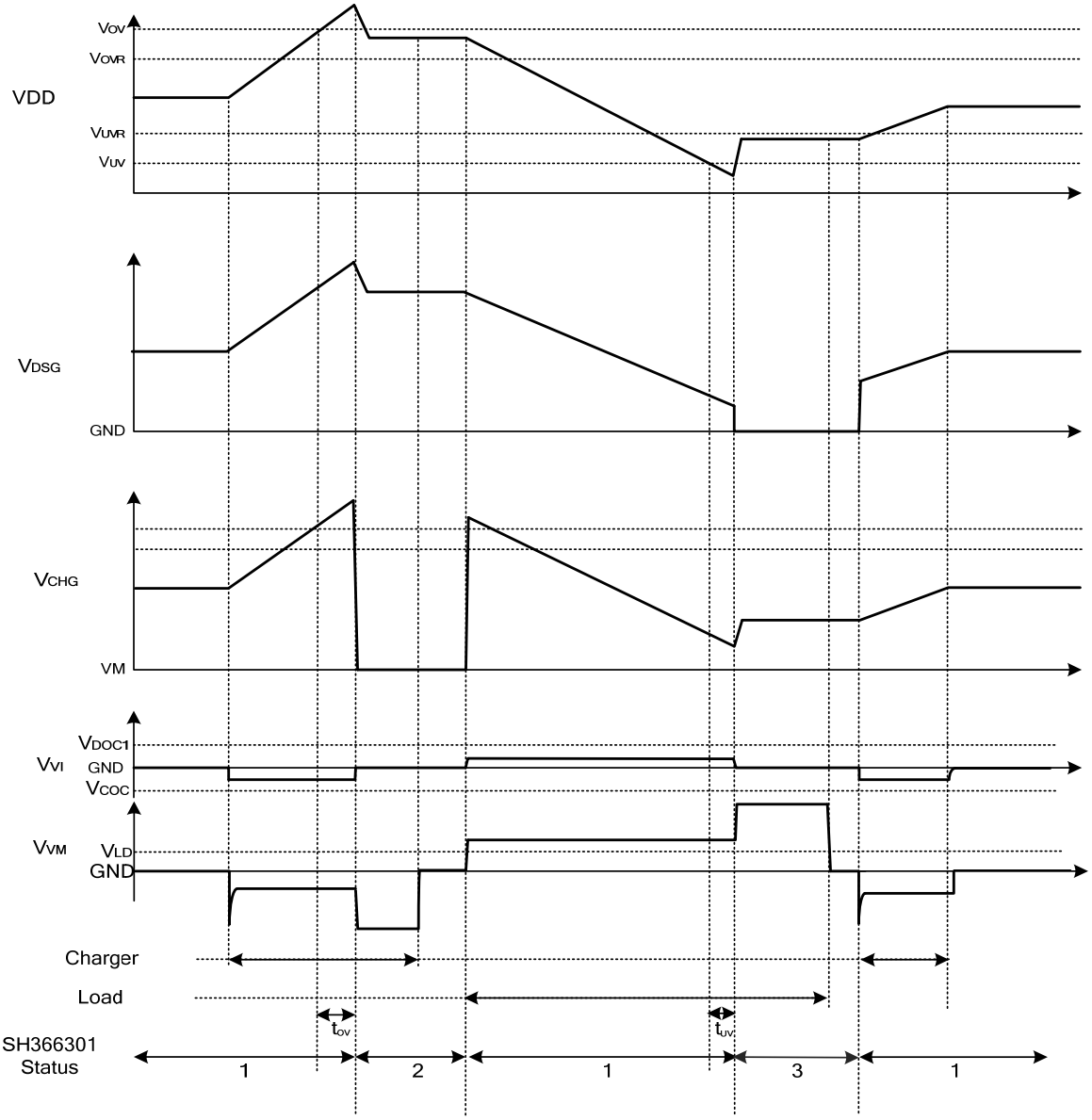
Fig 8. Application schematic of SH366301

8.2 External Components

	Symbol	Min.	Typ.	Max.	Unit
1	R_{vdd}	100	330	1000	Ω
2	C_{vdd}	0.068	0.1	1	μF
3	R_{vm}	100	470	1000	Ω
4	R_{Vi}	1	3	20	mΩ
5	R_{CTL}	-	1	-	kΩ

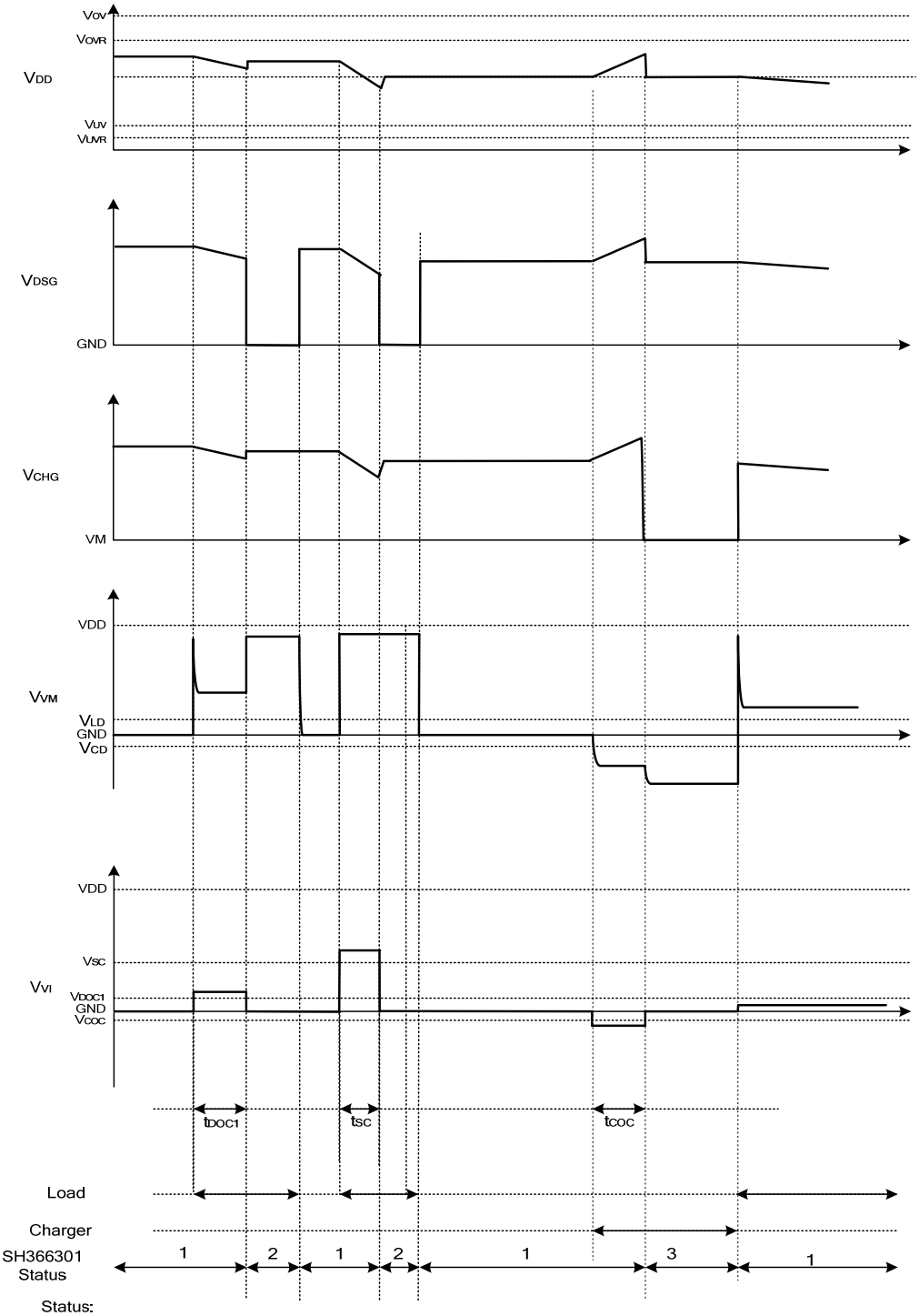
9 Timing Chart

9.1 Over-voltage and Under-voltage Chart



Status:
1.Normal status;
2.Over-charged status;
3.Over-discharged status;
tov:Delay time of over-charged detection;
tuv:Delay time of over-discharged detection;

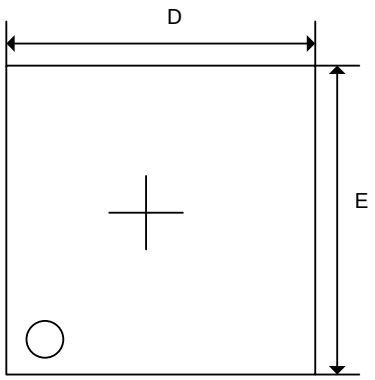
9.2 Over-current Operation Chart



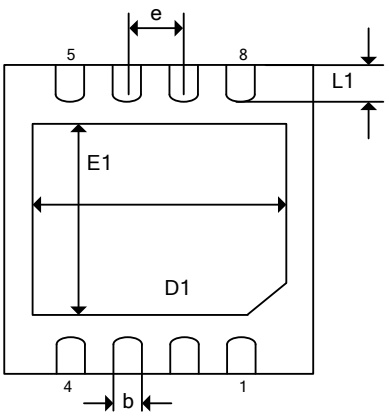
Status:
1.Normal status;
2.Discharging over-current status;
3.Charging over-current status;
t_{DOC1}/t_{COC}:Delay time of Discharging/Charging over-current;
t_{SC}:Delay time of short-circuit;

10 Package dimensions

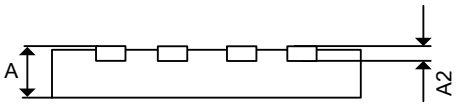
DFN 8L (1.6 X 1.6) (P0.40 T 0.55) Outline Dimensions **unit: mm**



Top View



Bottom View



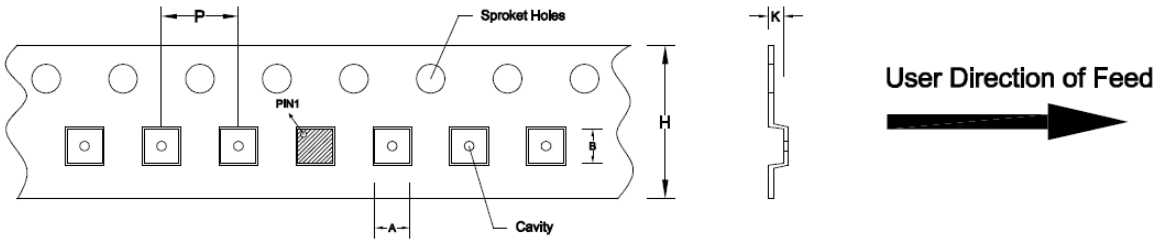
Side View

Symbol	Dimensions in mm		
	MIN	NOR	MAX
A	0.50	0.55	0.60
A2		0.152REF	
D	1.50	1.60	1.70
E	1.50	1.60	1.70
D1	1.30	1.40	1.50
E1	0.55	0.65	0.75
b	0.15	0.20	0.25
e		0.40TYP	
L1	0.15	0.20	0.25

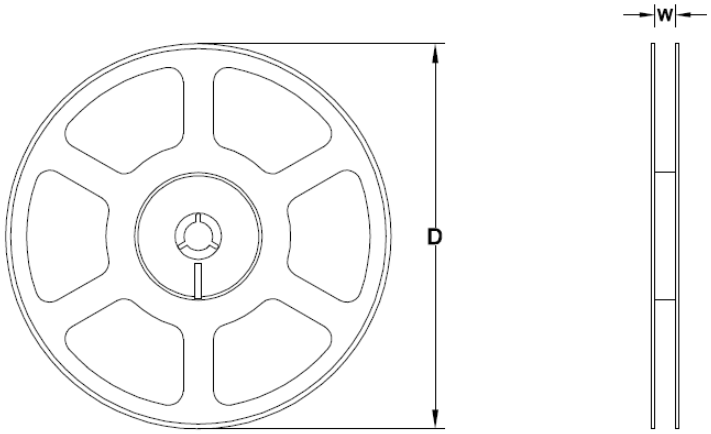
11 Carrier Tape and Reel Information

DFN8L (1.6*1.6) **unit : mm**

Carrier Tape Dimensions



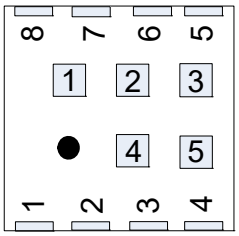
Reel Dimensions



*All dimensions are **nominal**

A	1.81	Dimension designed to accommodate the component width
B	1.81	Dimension designed to accommodate the component length
K	0.76	Dimension designed to accommodate the component thickness
H	8	Overall width of the carrier tape
P	4	Pitch between successive cavity centers
W	8.4	Reel width
D	178	Reel diameter

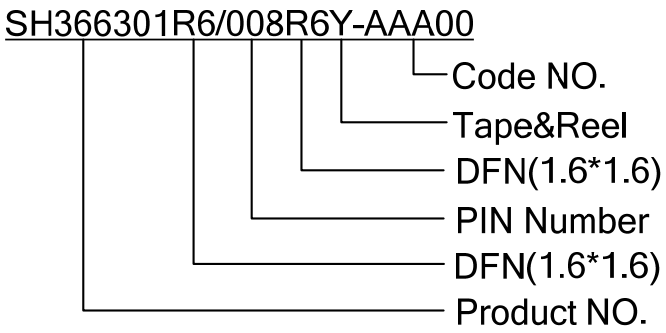
12 Mark Specification



Top view

①~③：Lot Number;
④~⑤：Product abbreviations(5A);

13 Product Name Structure



14 Modification record

Modification record of SH366301（AAA）		
Detailed description	**Located pages**	**Date**
Original version V0.0	-	2019/12/25
Remove the parameter I_{UV} in the sheet	P6/8/10	2020/07/16
Add the specific description about test circuit	P15/16/17/18	2020/07/16
Change the upper and lower limit of R_{VMS} in the sheet	P6/8/10	2020/09/14
Add the description about discharging short-circuit 2 V_{SC2}	P5/7/9/13/14	2020/09/14
Revise the test description and test circuit diagram	P14/15/16/17/18	2020/10/21
Change the test condition when measuring current consumption in over-discharged status	P15	2020/11/04
Add the typical,Max and Min value in the sheet	P5~P10	2020/11/20
Convert the parameters which reflect drive capability from I_{DH},I_{CH},I_{DL},I_{CL} to R_{DH},R_{CH}, R_{DL},R_{CL},meanwhile,revise the related test description.	P6/8/10/15	2020/12/23
Convert R_{DL} in the sheet from 0.5kΩ to 3.1kΩ@Typical	P6/8/10	2021/01/25
Revise the test description and test circuit diagram	P14/15/16/17/18	2021/02/24
Modify the test method of 7-1、7-2、7-12 and 7-13	P14/15	2022/06/09
Modify the related information of CTL voltage and add important notice at the end of the Datasheet	P6/8/10/13/15/25	2022/07/01
Revise the package dimensions	P22	2022/10/12
Modify the Test parameters of 7-23 、7-24 、 7-25、7-26	P16	2022/10/13

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