# SH366303R5/006R5Y-CAA00

CONTENTS

## 1 General Description

SH366303 is a protection IC for lithium-ion/ lithium polymer rechargeable batteries, including voltage detection circuits with strict accuracy and delay circuits. It aims for protecting 1-cell lithium-ion/ lithium polymer rechargeable battery packs from overcharged, overdischarged, and over-current status.

The SH366303 is a high voltage tolerance CMOS-based protection IC for rechargeable one-cell lithium-ion/ lithium polymer battery,aiming to detect over-charged/over-discharged status of one-cell Li+,along with excessive load current and charge current, protect the battery from the conditions described above. What's more,SH366303 contains short-circuit protector function to prevent excessive short-circuit current.

When the SH366303 detects over-charged voltage or charging over-current, the output of CHG pin switches to "L"(low) level after the internally fixed delay time. When the SH366303 detects over-discharged voltage or discharging over-current, the output of DSG pin switches to "L"(low) level after the internally fixed delay time.

After detecting over-charged voltage, the output of CHG can returns "H"(high) when one of the two following requirements is met:

(1)the cell voltage decreases lower than $V_{OVR}$ (over-charged release voltage);

(2)the cell voltage decreases lower than $V_{OV}$ (over-charged detection voltage),and a discharging current is detected (the load is connected to the circuit).

After detecting over-discharged voltage, the output of DSG pin returns to "H" when one of the two following requirements is met.

(1)The cell voltage increases higher than $V_{UVR}$ (over-discharged release voltage);

(2) the cell voltage gets higher than $V_{UV}$ (over-discharged detection voltage),and a charger is connected.

When the charging over-current is detected,SH366303 will quit the charging over-current status and CHG returns to "H" level if the load circuit is connected.

When the discharging over-current or short-circuit current is detected, SH366303 will quit the discharging over-current or short-circuit status and DSG pin returns to "H" level if the load circuit is removed.

| **Part.No** | $V_{OV}$ **(V)** | $V_{OVR}$ **(V)** | $V_{UV}$ **(V)** | $V_{UVR}$ **(V)** | $V_{DOC1}$ **(mV)** | $V_{SC}$ **(mV)** | $V_{COC}$ **(mV)** | 0V battery Charge **(Allowed/Forbidden )** |
|---|---|---|---|---|---|---|---|---|
| SH366303R5/006R5Y-CAA00 | 4.470 | 4.275 | 2.500 | 2.700 | 60 | 190 | -60 | Forbidden |

| **Part.No** | $t_{OV}$ **(s)** | $t_{UV}$ **(ms)** | $t_{DOC1}$ **(ms)** | $t_{SC}$ **(μs)** | $t_{COC}$ **(ms)** | Power Down Mode **(YES/NO)** |
|---|---|---|---|---|---|---|
| SH366303R5/006R5Y-CAA00 | 1.0 | 32 | 16 | 280 | 8 | YES |

## 2 Block Diagram

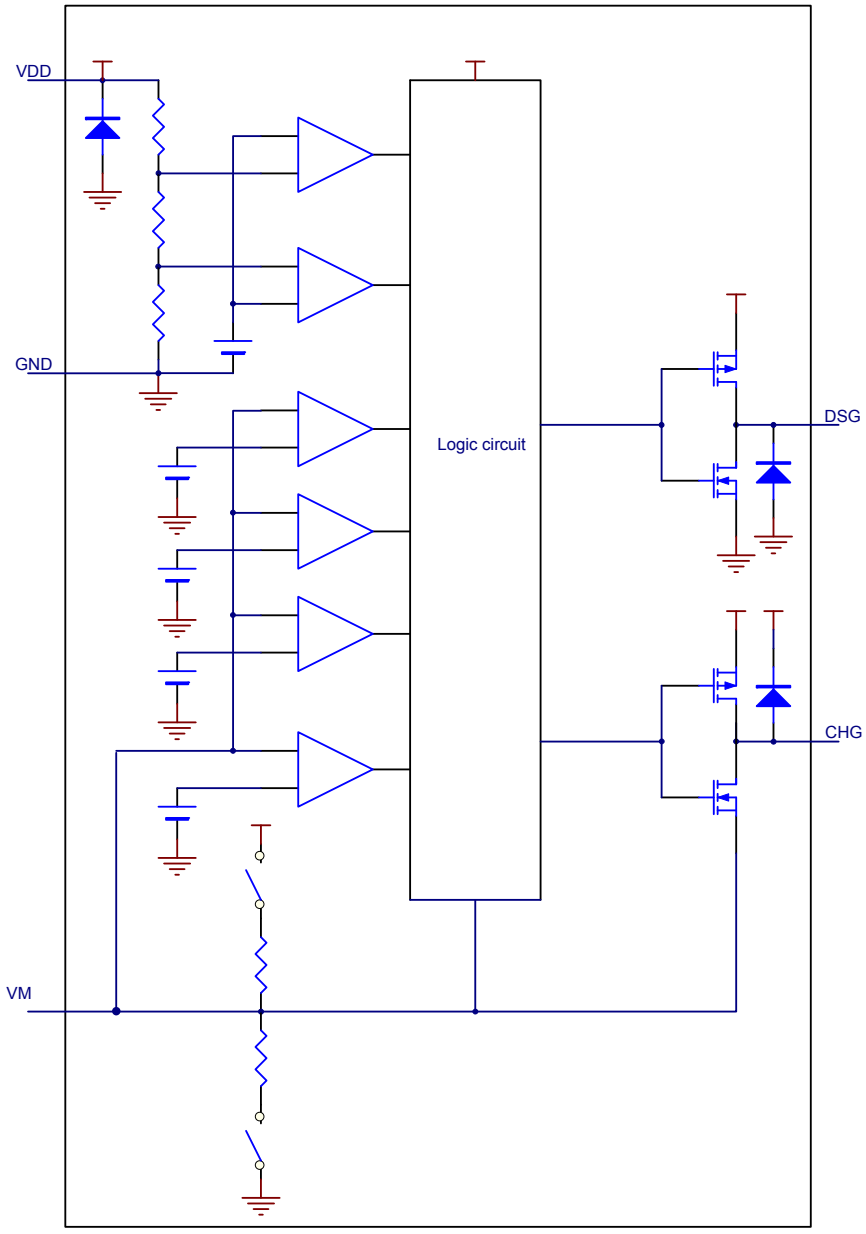



**Fig 1. SH366303 Block Diagram**

## 3 Pin Descriptions

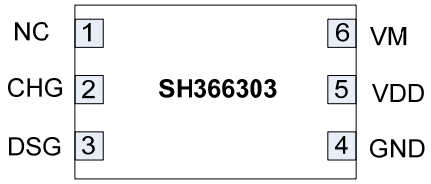



**Fig 2. Pin Configuration of SH366303**

**Table1. SH366303 pin description (Total 6 pins.)**

| Pin NO. | Pin Name | I/O | Function Description |
|---|---|---|---|
| 1 | NC | - | No connection； |
| 2 | CHG | O | Drive pin of charge MOSFET; |
| 3 | DSG | O | Drive pin of discharge MOSFET; |
| 4 | GND | I | Input pin for negative power supply; |
| 5 | VDD | I | Input pin for positive power supply; |
| 6 | VM | I | Load and charger detection pin/Current detection pin; |

## 4 Absolute maximum ratings

(Ta=25°C,GND=0V)

| Item | Pin Name | Absolute maximum ratings | Unit |
|---|---|---|---|
| Input voltage between VDD pin and GND pin | VDD | GND-0.3 to GND+6.0 | V |
| VM pin input voltage | VM | VDD-28 to VDD+0.3 | V |
| CHG pin output voltage | CHG | $V_{VM}$-0.3 to VDD+0.3 | V |
| DSG pin output voltage | DSG | GND-0.3 to VDD+0.3 | V |
| Operation ambient temperature | - | -40 to 85 | °C |
| Storage temperature | - | -40 to 125 | °C |

***Note1：*** ***If the actual operating parameter exceeds the range of absolute maximum ratings,the components of SH366303 will be permanently damaged. Only when the operating parameters are among the regulated range above, the relevant functions can be guaranteed in normal working status.***

## 5 Electrical characteristics

### 5.1 Electrical characteristics(unless otherwise specified, Ta=25°C)

| Symbol | Item | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|
| $V_{OV}$ | Overcharge detection voltage(25°C) | 4.450 | 4.470 | 4.490 | V | A |
| | Overcharge detection voltage(0°C~60°C) | 4.450 | 4.470 | 4.495 | V | A |
| $V_{OVR}$ | Overcharge release voltage | 4.225 | 4.275 | 4.325 | V | A |
| $t_{OV}$ | Overcharge detection delay time | 0.7 | 1.0 | 1.3 | s | B |
| $t_{OVR}$ | Overcharge release delay time | 0.65 | 1.0 | 1.5 | ms | B |
| $t_{OVHR}$ | Overcharge hysteresis release delay time | 150 | 250 | 500 | μs | B |
| $V_{UV}$ | Overdischarge detection voltage | 2.450 | 2.500 | 2.550 | V | A |
| $V_{UVR}$ | Overdischarge release voltage | 2.625 | 2.700 | 2.775 | V | A |
| $t_{UV}$ | Overdischarge detection delay time | 22.4 | 32.0 | 41.6 | ms | B |
| $t_{UVR}$ | Overdischarge release delay time | 0.7 | 5.0 | 11.7 | ms | B |
| $t_{UVHR}$ | Overdischarge hysteresis release delay time | 0.65 | 1.0 | 1.5 | ms | B |
| $t_{PD}$ | delay time of entering Power Down Mode | 0.4 | 1.0 | 2.5 | ms | B |
| $t_{PDR}$ | delay time of quitting Power Down Mode | 0.7 | 1.0 | 1.3 | ms | B |
| $V_{DOC1}$ | Discharge overcurrent 1 detection voltage | 55 | 60 | 65 | mV | B |
| $t_{DOC1}$ | Discharge overcurrent 1 detection delay time | 11.2 | 16.0 | 20.8 | ms | B |
| $V_{SC}$ | Short circuit detection voltage | 150 | 190 | 230 | mV | B |
| $t_{SC}$ | Short circuit detection delay time | 196 | 280 | 364 | μs | B |
| $V_{DOCR}$ | Discharge overcurrent release voltage | 0.78*VDD | 0.83*VDD | 0.86*VDD | V | B |
| $t_{DOCR}$ | Discharge overcurrent release delay time | 0.65 | 1.0 | 1.5 | ms | B |
| $V_{COC}$ | Charge overcurrent detection voltage | -65 | -60 | -55 | mV | B |
| $t_{COC}$ | Charge overcurrent detection delay time | 5.6 | 8.0 | 10.4 | ms | B |
| $t_{COCR}$ | Charge overcurrent release delay time | 160 | 250 | 375 | μs | B |

| Symbol | Item | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|
| $V_{CHGH}$ | CHG output high voltage | VDD-0.15 | VDD-0.02 | VDD | V | F |
| $V_{DSGH}$ | DSG output high voltage | VDD-0.15 | VDD-0.02 | VDD | V | F |
| $V_{LD}$ | Load detection voltage | 0.3 | 0.35 | 0.4 | V | B |
| $V_{CD1}$ | Charger detection voltage | GND-0.01 | GND | GND+0.01 | V | B |
| $V_{CD2}$ | Charger detection voltage 2 | 0.6 | 0.7 | 1.2 | V | B |
| $V_{0INH}$ | Minimum battery voltage for charging | 0.9 | 1.5 | 1.7 | V | B |
| $I_{CC}$ | Operating current (VDD=3.4V) | 1 | 2 | 3 | μA | C |
| | Operating current (VDD=4.4V) | 1 | 2 | 3 | μA | C |
| $I_{PD}$ | Current consumption of sleep status(VDD=1.5V) | 0.01 | 0.03 | 0.05 | μA | C |
| $R_{DH}$ | Internal pull-up resistance of DSG pin | 0.5 | 1.0 | 1.7 | kΩ | D |
| $R_{CH}$ | Internal pull-up resistance of CHG pin | 1.2 | 2.5 | 5.0 | kΩ | D |
| $R_{DL}$ | Internal pull-down resistance of DSG pin | 2.1 | 3.1 | 4.1 | kΩ | D |
| $R_{CL}$ | Internal pull-down resistance of CHG pin | 1.6 | 2.5 | 4.0 | kΩ | D |
| $t_{DH}$ | The time during the period that the DSG pin rises from GND to VDD-0.5 | 3 | 8 | 15 | μs | E |
| $t_{DL}$ | The time during the period that the DSG pin decreases from VDD-0.5 to GND | 10 | 35 | 100 | μs | E |
| $t_{CH}$ | The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5 | 10 | 25 | 40 | μs | E |
| $t_{CL}$ | The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM | 15 | 47 | 60 | μs | E |
| $R_{VMS}$ | Internal pull-down resistance of VM pin | 7.5 | 10 | 15 | kΩ | C |
| $R_{VMD}$ | Internal pull-up resistance of VM pin | 0.5 | 1.25 | 2.5 | MΩ | C |

### 5.2 Electrical characteristics(unless otherwise specified, Ta=-25°C~70°C)

| Symbol | Item | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|
| $V_{OV}$ | Overcharge detection voltage | 4.445 | 4.470 | 4.495 | V | A |
| $V_{OVR}$ | Overcharge release voltage | 4.220 | 4.275 | 4.330 | V | A |
| $t_{OV}$ | Overcharge detection delay time | 0.6 | 1.0 | 1.4 | s | B |
| $t_{OVR}$ | Overcharge release delay time | 0.5 | 1.0 | 2.0 | ms | B |
| $t_{OVHR}$ | Overcharge hysteresis release delay time | 125 | 250 | 500 | μs | B |
| $V_{UV}$ | Overdischarge detection voltage | 2.445 | 2.500 | 2.555 | V | A |
| $V_{UVR}$ | Overdischarge release voltage | 2.615 | 2.700 | 2.785 | V | A |
| $t_{UV}$ | Overdischarge detection delay time | 19.2 | 32.0 | 44.8 | ms | B |
| $t_{UVR}$ | Overdischarge release delay time | 0.6 | 5.0 | 12.6 | ms | B |
| $t_{UVHR}$ | Overdischarge hysteresis release delay time | 0.5 | 1.0 | 2.0 | ms | B |
| $t_{PD}$ | delay time of entering Power Down Mode | 0.6 | 1.0 | 1.4 | ms | B |
| $t_{PDR}$ | delay time of quitting Power Down Mode | 0.6 | 1.0 | 1.4 | ms | B |
| $V_{DOC1}$ | Discharge overcurrent 1 detection voltage | 55 | 60 | 65 | mV | B |
| $t_{DOC1}$ | Discharge overcurrent 1 detection delay time | 10.4 | 16.0 | 21.6 | ms | B |
| $V_{SC}$ | Short circuit detection voltage | 150 | 190 | 230 | mV | B |
| $t_{SC}$ | Short circuit detection delay time | 168 | 280 | 392 | μs | B |
| $V_{DOCR}$ | Discharge overcurrent release voltage | 0.78*VDD | 0.83*VDD | 0.86*VDD | V | B |
| $t_{DOCR}$ | Discharge overcurrent release delay time | 0.5 | 1.0 | 2.0 | ms | B |
| $V_{COC}$ | Charge overcurrent detection voltage | -65 | -60 | -55 | mV | B |
| $t_{COC}$ | Charge overcurrent detection delay time | 4.8 | 8.0 | 11.2 | ms | B |
| $t_{COCR}$ | Charge overcurrent release delay time | 125 | 250 | 500 | μs | B |

| Symbol | Item | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|
| $V_{CHGH}$ | CHG output high voltage | VDD-0.15 | VDD-0.02 | VDD | V | F |
| $V_{DSGH}$ | DSG output high voltage | VDD-0.15 | VDD-0.02 | VDD | V | F |
| $V_{LD}$ | Load detection voltage | 0.3 | 0.35 | 0.4 | V | B |
| $V_{CD1}$ | Charger detection voltage | GND-0.01 | GND | GND+0.01 | | B |
| $V_{CD2}$ | Charger detection voltage 2 | 0.6 | 0.7 | 1.2 | V | B |
| $V_{0INH}$ | Minimum battery voltage for charging | 0.7 | 1.5 | 1.8 | V | B |
| $I_{CC}$ | Operating current (VDD=3.4V) | 1 | 2 | 4 | μA | C |
| | Operating current (VDD=4.4V) | 1 | 2 | 4 | μA | C |
| $I_{PD}$ | Current consumption of sleep status(VDD=1.5V) | 0.01 | 0.03 | 0.1 | μA | C |
| $R_{DH}$ | Internal pull-up resistance of DSG pin | 0.5 | 1.0 | 1.7 | kΩ | D |
| $R_{CH}$ | Internal pull-up resistance of CHG pin | 1.2 | 2.5 | 5.0 | kΩ | D |
| $R_{DL}$ | Internal pull-down resistance of DSG pin | 2.1 | 3.1 | 4.1 | kΩ | D |
| $R_{CL}$ | Internal pull-down resistance of CHG pin | 1.6 | 2.5 | 4.0 | kΩ | D |
| $t_{DH}$ | The time during the period that the DSG pin rises from GND to VDD-0.5 | 3 | 8 | 15 | μs | E |
| $t_{DL}$ | The time during the period that the DSG pin decreases from VDD-0.5 to GND | 10 | 35 | 100 | μs | E |
| $t_{CH}$ | The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5 | 10 | 25 | 40 | μs | E |
| $t_{CL}$ | The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM | 15 | 47 | 60 | μs | E |
| $R_{VMS}$ | Internal pull-down resistance of VM pin | 7.5 | 10 | 15 | kΩ | C |
| $R_{VMD}$ | Internal pull-up resistance of VM pin | 0.25 | 1.25 | 3.50 | MΩ | C |

### 5.3 Electrical characteristics(unless otherwise specified, Ta=-40°C~85°C)

| Symbol | Item | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|
| $V_{OV}$ | Overcharge detection voltage | 4.435 | 4.470 | 4.505 | V | A |
| $V_{OVR}$ | Overcharge release voltage | 4.215 | 4.275 | 4.335 | V | A |
| $t_{OV}$ | Overcharge detection delay time | 0.5 | 1.0 | 1.5 | s | B |
| $t_{OVR}$ | Overcharge release delay time | 0.5 | 1.0 | 2.0 | ms | B |
| $t_{OVHR}$ | Overcharge hysteresis release delay time | 125 | 250 | 500 | μs | B |
| $V_{UV}$ | Overdischarge detection voltage | 2.420 | 2.500 | 2.580 | V | A |
| $V_{UVR}$ | Overdischarge release voltage | 2.600 | 2.700 | 2.800 | V | A |
| $t_{UV}$ | Overdischarge detection delay time | 16 | 32 | 48 | ms | B |
| $t_{UVR}$ | Overdischarge release delay time | 0.5 | 5.0 | 13.5 | ms | B |
| $t_{UVHR}$ | Overdischarge hysteresis release delay time | 0.5 | 1.0 | 2.0 | ms | B |
| $t_{PD}$ | delay time of entering Power Down Mode | 0.5 | 1.0 | 1.5 | ms | B |
| $t_{PDR}$ | delay time of quitting Power Down Mode | 0.5 | 1.0 | 1.5 | ms | B |
| $V_{DOC1}$ | Discharge overcurrent 1 detection voltage | 55 | 60 | 65 | mV | B |
| $t_{DOC1}$ | Discharge overcurrent 1 detection delay time | 8.0 | 16.0 | 24.0 | ms | B |
| $V_{SC}$ | Short circuit detection voltage | 150 | 190 | 230 | mV | B |
| $t_{SC}$ | Short circuit detection delay time | 140 | 280 | 420 | μs | B |
| $V_{DOCR}$ | Discharge overcurrent release voltage | 0.78*VDD | 0.83*VDD | 0.86*VDD | V | B |
| $t_{DOCR}$ | Discharge overcurrent release delay time | 0.5 | 1.0 | 2.0 | ms | B |
| $V_{COC}$ | Charge overcurrent detection voltage | -65 | -60 | -55 | mV | B |
| $t_{COC}$ | Charge overcurrent detection delay time | 4 | 8 | 12 | ms | B |
| $t_{COCR}$ | Charge overcurrent release delay time | 125 | 250 | 500 | μs | B |

| Symbol | Item | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|
| $V_{CHGH}$ | CHG output high voltage | VDD-0.15 | VDD-0.02 | VDD | V | F |
| $V_{DSGH}$ | DSG output high voltage | VDD-0.15 | VDD-0.02 | VDD | V | F |
| $V_{LD}$ | Load detection voltage | 0.30 | 0.35 | 0.40 | V | B |
| $V_{CD1}$ | Charger detection voltage | GND-0.01 | GND | GND+0.01 | V | B |
| $V_{CD2}$ | Charger detection voltage 2 | 0.6 | 0.7 | 1.2 | V | B |
| $V_{0INH}$ | Minimum battery voltage for charging | 0.7 | 1.5 | 1.8 | V | B |
| $I_{CC}$ | Operating current (VDD=3.4V) | 1 | 2 | 4 | μA | C |
| | Operating current (VDD=4.4V) | 1 | 2 | 4 | μA | C |
| $I_{PD}$ | Current consumption of sleep status(VDD=1.5V) | 0.01 | 0.03 | 0.1 | μA | C |
| $R_{DH}$ | Internal pull-up resistance of DSG pin | 0.5 | 1.0 | 1.7 | kΩ | D |
| $R_{CH}$ | Internal pull-up resistance of CHG pin | 1.2 | 2.5 | 5.0 | kΩ | D |
| $R_{DL}$ | Internal pull-down resistance of DSG pin | 2.1 | 3.1 | 4.1 | kΩ | D |
| $R_{CL}$ | Internal pull-down resistance of CHG pin | 1.6 | 2.5 | 4.0 | kΩ | D |
| $t_{DH}$ | The time during the period that the DSG pin rises from GND to VDD-0.5 | 3 | 8 | 15 | μs | E |
| $t_{DL}$ | The time during the period that the DSG pin decreases from VDD-0.5 to GND | 10 | 35 | 100 | μs | E |
| $t_{CH}$ | The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5 | 10 | 25 | 40 | μs | E |
| $t_{CL}$ | The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM | 15 | 47 | 60 | μs | E |
| $R_{VMS}$ | Internal pull-down resistance of VM pin | 7.5 | 10 | 15 | kΩ | C |
| $R_{VMD}$ | Internal pull-up resistance of VM pin | 0.25 | 1.25 | 3.5 | MΩ | C |

***Note2：*** ***The current flowing into the chip is negative, such as leak current. The current flowing out of the chip is positive, such as power consumption, pull current.***

***Note3：*** ***Refer to test circuits in chapter 7.***

## 6 Function Description

### 6.1 Normal status

When all the following conditions are satisfied, SH366303 is in normal status:

(1). The battery voltage is between $V_{UV}$(over-discharged detection voltage) and $V_{OV}$(over-charged detection voltage);

(2). The VM pin voltage of SH366303 is between $V_{COC}$(charging over-current detection voltage) and $V_{DOC1}$ (discharging over-current 1 detection voltage);

(3). CHG pin outputs VDD, DSG pin outputs VDD,charge and discharge MOSFET are both turned on.

### 6.2 Over-charged status

When all the following conditions are satisfied, SH366303 enters over-charged status and turns off the charge MOSFET:

(1). The battery voltage is higher than $V_{OV}$ (over-charged detection voltage);

(2). The condition of (1) lasts up to $t_{OV}$ (over-charged detection delay time) or longer;

When one of the following conditions is satisfied, the over-charged status is released, and the charge MOSFET is turned on:

(1). The voltage of the VM pin is lower than $V_{LD}$(without load connection), and the cell voltage is lower than $V_{OVR}$ (over-charged release voltage),lasting up to $t_{OVR}$ (over-charged release delay time) or longer;

(2). The voltage of the VM pin is higher than $V_{LD}$ (with load connection), lasting up to $t_{OVHR}$ (over-charged release hysteresis delay time) or longer, and the cell voltage is lower than $V_{OV}$ (over-charged detection voltage);

***Note4：*** ***When SH366303 is in overcharge status,the discharging over-current detection and short-circuit detection function is disabled.***

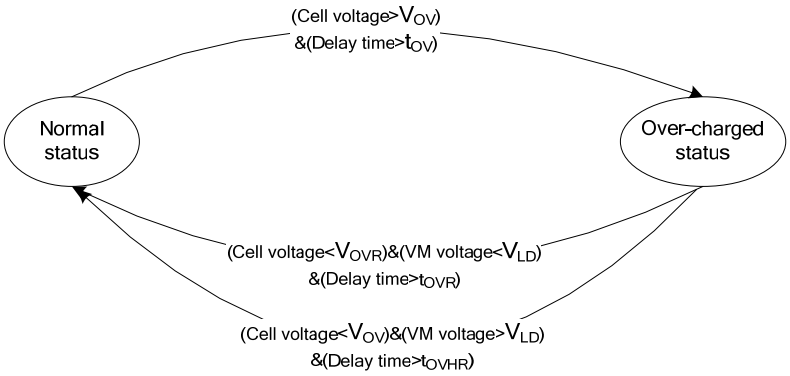



**Fig 3. Over-charged Protection**

### 6.3 Over-discharged status

When all the following conditions are satisfied, SH366303 enters over-discharged status and turns off the discharge MOSFET,the internal pull-up resistance is also turned on:

(1). The cell voltage is lower than $V_{UV}$(over-discharged detection voltage);

(2). The condition (1) lasts up to $t_{UV}$ (over-discharged detection delay time) or longer;

When one of the following conditions is satisfied, the over-discharged status is released, and the discharge MOSFET is turned on:

(1). The voltage of the VM pin is not lower than $V_{CD1}$ (without charger plugged in), and the cell voltage is higher than $V_{UVR}$ ,lasting up to $t_{UVR}$(delay time of over-discharged release detection);

(2). The voltage of the VM pin is lower than $V_{CD1}$ (with charger plugged in),lasting up to $t_{UVHR}$ (delay time of over-discharged release hysteresis) or longer, and the cell voltage is higher than $V_{UV}$(over-discharged detection voltage);

***Note5：*** ***When cell voltage is lower than $V_{UV}$,the charging overcurrent detection function is disabled.***

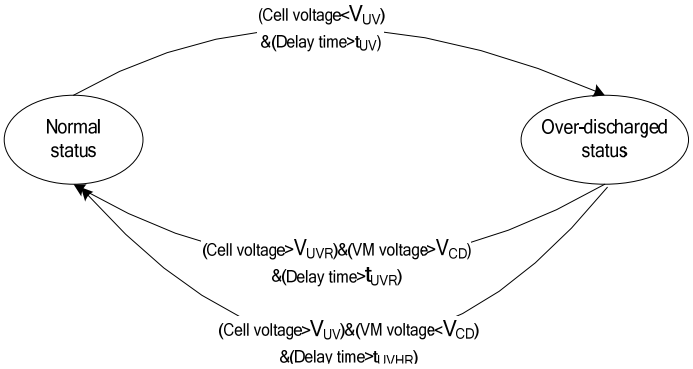



**Fig 4. Over-discharged Protection**

### 6.4 Power Down satus

When the system is over-discharged,SH366303 will enter Power Down status when all the following conditions are satisfied,and the internal pull-up resistance of SH366303 is turned on:

(1). The voltage of VM pin is higher than VDD-0.8;

(2). The condition of (1) lasts for longer than $t_{PD}$ (delay time of entering power down status ).

When system is in Power Downstatus,SH366303 will quit the Power Downstatus when all the following conditions are satisfied,and the system enters into over-discharged status.

(1).The voltage of VM pin is lower than $V_{CD2}$(typical value of charger detection voltage2);

(2).The condition of (1) lasts for longer than $t_{PDR}$ (delay time of quitting power down state ).

### 6.5 Discharging over-current status

SH366303 has two levels for discharging over-current protection, $V_{DOC1}$ (discharging over-current 1 detection voltage) is lower than $V_{SC}$(short-circuit detection voltage), $t_{DOC1}$ (delay time of discharging over-current detection 1) is larger than $t_{SC}$ (short-circuit detection delay time).

When all the following conditions are satisfied, SH366303 enters discharging over-current status and turns off the discharge MOSFET:

(1). The VM pin voltage of SH366303 is higher than $V_{DOC1}$/ $V_{SC}$;

(2). The condition of (1) lasts up to $t_{DOC1}$ / $t_{SC}$ or longer;

When all the following conditions are satisfied, the discharging over-current status is released:

(1). Load is disconnected or charger is connected(the VM voltage is lower than $V_{DOCR}$);

(2). The condition of (1) lasts up to the $t_{DOCR}$ (delay time of discharging over-current release) or longer.

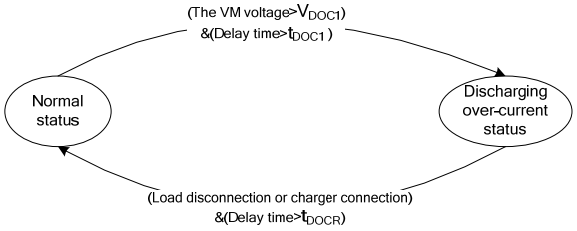



**Fig 5. Discharging over-current 1 Protection**

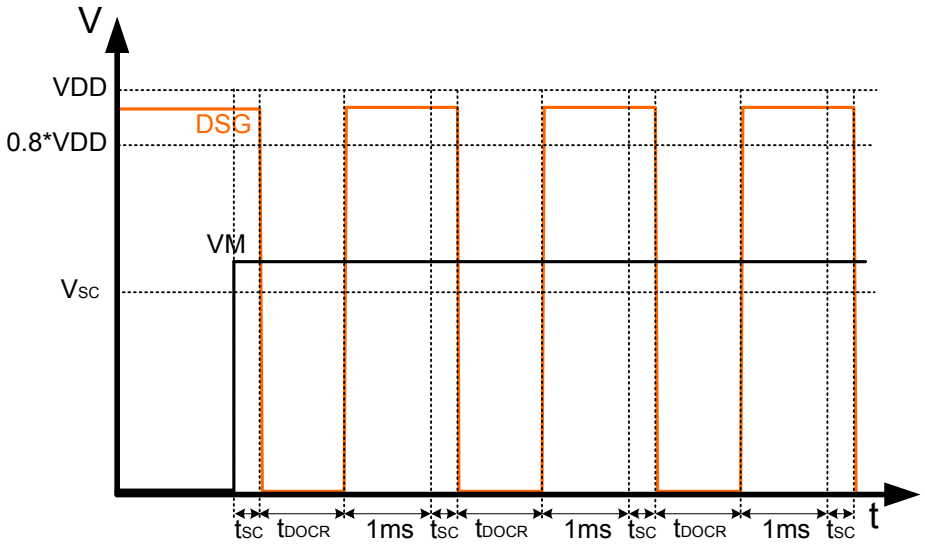



**Fig 5-1. Discharging over-current release**

***Note6：*** ***When SH366303 is in discharging over-current status, SH366303 will turn on the internal pull-down resistance and pull VM pin down to GND,in order to judge whether the outside load is removed. After the status in which DSG pin returns high after $t_{DOCR}$,system won't detect discharging over-current within 1ms,so DSG pin keeps high among this period(refer to Fig 5-1).***

### 6.6 Charging over-current status

SH366303 contains charging over-current protection funtion, when all the following conditions are satisfied, system enters charging over-current status and turns off the charge MOSFET:

(1). The VM pin voltage of SH366303 is lower than $V_{COC}$(charging over-current detection voltage);

(2). The condition of (1) lasts longer than $t_{COC}$(delay time of charging over-current detection);

When all the following conditions are satisfied, the charging over-current status is released:

(1). The load is connected (the voltage of the VM pin is higher than $V_{LD}$);

(2). The condition of (1) lasts longer than $t_{COCR}$(delay time of charging over-current release);

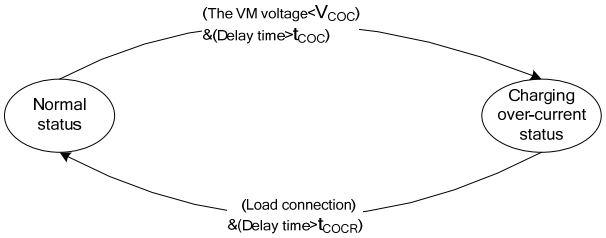



**Fig 6. Charging over-current Protection**

### 6.7 Function for 0V battery

When the battery voltage decreases lower than $V_{0INH}$, the charge MOSFET will be turned off to inhibit charging.

## 7 Test Circuits

7-1. Overcharge detection voltage ($V_{OV}$) & Overcharge release voltage($V_{OVR}$)

【Test Circuit】: A

【Description】: Set V1=3.4V,connect VM to GND.Increase V1 until the voltage of CHG pin drop to low,the present V1 is $V_{OV}$.Then decrease V1 from present voltage,until the voltage of CHG pin returns to normal,similarly,is $V_{OVR}$.

7-2. Overdischarge detection voltage ($V_{UV}$) & Overdischarge release voltage ($V_{UVR}$)

【Test Circuit】: A

【Description】: Set V1=3.4V,connect VM to GND.Decrease V1 until the voltage of DSG pin drop to low, the present V1 is $V_{UV}$ .Then Increase V1 from present voltage,until DSG pin returns to normal,similarly,is $V_{UVR}$ .

7-3. Discharge overcurrent 1 detection voltage ($V_{DOC1}$)

【Test Circuit】: B

【Description】: Set V1=VDD-1=3.4V,V2=0V,connect switch1.Increase V2 until the following two requirements are satisfied.Then,the present V2 is $V_{DOC1}$.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V2 and shutting down of DSG is aroud 16ms.

7-4. Short circuit detection voltage($V_{SC}$)

【Test Circuit】: B

【Description】: Set V1= VDD-1=3.4V, V2=0V, connect switch1.Increase V2 until the following two requirements are satisfied.Then,the present V2 is $V_{SC}$.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V2 and shutting down of DSG is aroud 280μs.

7-5. Discharge overcurrent release voltage ($V_{DOCR}$)

【Test Circuit】: B

【Description】: Set V1= VDD-1=3.4V,V2=3.4V,connect switch1,DSG turns low.Then disconnect VM from V2,then decrease VDD-1 till DSG returns high(the approximate point is 0.8*V1).The present V2 is $V_{DOCR}$.

7-6. Charge overcurrent detection voltage ($V_{COC}$)

【Test Circuit】: B

【Description】: Set V1=3.4V,V2= 0V,disconnect VDD-1 and switch1.Decrease V2 until CHG pin shuts down.Then,the present V2 is $V_{COC}$.

7-7. Load detection voltage ($V_{LD}$)

【Test Circuit】: B

【Description】: Set V1=4.7V,V2= 0V,disconnect VDD-1 and switch1,the CHG pin turns low,then decrease V1 to 4.45V .Increase V2 till the point where CHG returns high.The present V2 is $V_{LD}$.

7-8. Charger detection voltage ($V_{CD1}$)

【Test Circuit】: B

【Description】: Set V1=2.4V, V2=0.1V,disconnect VDD-1 and switch1,the DSG pin turns low.Then increase V1=2.6V.Decrease V2 gradually,if V2 is decreased to 0V while DSG still keeps low,then continue decrease V2 to negative( adjustment step is 1mV),till the DSG returns high.The present V2 is the $V_{CD1}$.

7-9．Charger detection voltage 2($V_{CD2}$)

【Test Circuit】：B

【Description】：Set V1=V2=2.4V,disconnect VDD-1 and switch1,the DSG pin turns low.Then increase V1=2.8V.Decrease V2 gradually till the DSG returns high.The present V2 is the $V_{CD2}$.

7-10．Operating current in normal mode($I_{CC}$)

【Test Circuit】：C

【Description】：Set V1=3.4V,V2=0.Record the current at IC's VDD pin.

7-11．Current consumption of over-discharged status ($I_{PD}$)

【Test Circuit】：C

【Description】：Set V1=V2=1.8V.Record the current at IC's VDD pin,which is $I_{PD.}$

7-12．Internal pull-down resistance of VM pin ($R_{VMS}$)

【Test Circuit】：C

【Description】：Set VDD= V2=3.4V,DSG pin turns low.Record the current at IC's VM pin $I_{VM}$,then calculate the result: $R_{VMS}$=3.4V/ $I_{VM}$.

7-13．Internal pull-up resistance of VM pin ($R_{VMD}$)

【Test Circuit】：C

【Description】：Set V1=2.4V, V2= 0V.Record the current at IC's VM pin $I_{VM}$,and calculate the $R_{VMD}=V1/I_{VM}$.

7-14．Internal pull-up resistance of DSG pin ($R_{DH}$)

【Test Circuit】：D

【Description】：Set V1=4.0V,V2=V5=0V,V3=V4=3.5V,obtain the current flowing out the DSG pin $I_{DO}$.$R_{DH}$=0.5V/ $I_{DO.}$

7-15．Internal pull-up resistance of CHG pin ($R_{CH}$)

【Test Circuit】：D

【Description】：Set V1=4.0V,V2=V5=0V,V3=V4=3.5V,obtain the current flowing out the CHG pin $I_{CO}$. $R_{CH}$=0.5V/ $I_{CO.}$

7-16．Internal pull-down resistance of DSG pin ($R_{DL}$)

【Test Circuit】：D

【Description】：Set VDD=2.2V,V2=V5=0V,V4=0.1V,system enter over-discharge protection system and DSG pin turns down.Obtain the current sinking into the DSG pin $I_{CO}$.$R_{DL}$=0.5V/ $I_{CO.}$

7-17．Internal pull-down resistance of CHG pin ($R_{CL}$)

【Test Circuit】：D

【Description】：Set VDD=4.7V,V2=V5=0V,V3=0.1V,system enter over-charge protection system and CHG pin turns down.Obtain the current sinking into the CHG pin $I_{CO}$.$R_{DL}$=0.5V/ $I_{CO.}$

7-18．Overcharge detection delay time ($t_{OV}$)

【Test Circuit】：B

【Description】：Set V1=3.4V, V2 =0V, disconnect VDD-1 and switch1,system operates in normal status.Then change V1 swiftly to 4.7V,the delay time between the point where V1 is higher than the actual $V_{OV}$ and shutting down of CHG is exactly the $t_{OV}$.

7-19．Overdischarge detection delay time ($t_{UV}$)

【Test Circuit】：B

【Description】：Set V1=3.4V, V2= 0V, disconnect VDD-1 and switch1,system operates in normal status.Then change V1 swiftly to 2.4V,the delay time between the point where V1 is lower than the actual $V_{UV}$ and shutting down of DSG is exactly the $t_{UV}$.

7-20．Discharge overcurrent 1 detection delay time ($t_{DOC1}$)

【Test Circuit】：B

【Description】：Set V1=VDD-1=3.4V,V2=0V, connect switch1,system operates in normal status.Set V2=65mV,connect VM to V2 swiftly,the delay time between the rise of VM and shutting down of DSG is exactly the $t_{DOC1.}$

7-21．Short circuit detection voltage ($t_{SC}$)

【Test Circuit】：B

【Description】：Set V1= VDD-1=3.4V,V2=0V,connect switch1,system operates in normal status.Set V2=230mV,connect VM to V2 swiftly,the delay time between the rise of VM and shutting down of DSG is exactly the $t_{SC.}$

7-22．Charge overcurrent detection delay time ($t_{COC}$)

【Test Circuit】：B

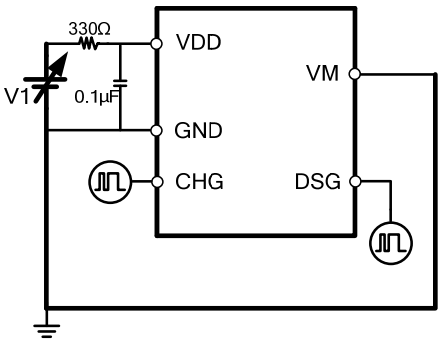
【Description】：Set V1=3.4V,V2=-2mV,disconnect VDD-1 and switch1,system operates in normal status.Set V2=-65mV,connect VM to V2 swiftly,the delay time between the drop of VM and shutting down of CHG is exactly the $t_{COC.}$

7-23．Minimum charger voltage ($V_{0INH}$)

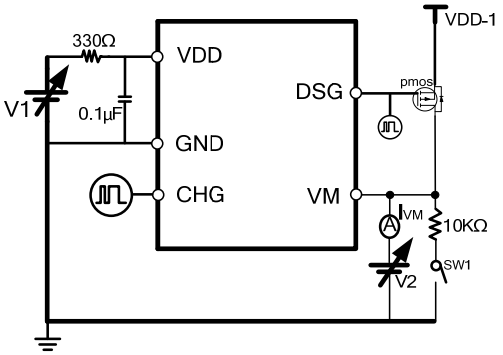
【Test Circuit】：B

【Description】：Set V1=1.9V,V2 =0V,disconnect VDD-1 and switch1.Decrease V1 till the point where CHG turns down.The present V1 is $V_{0INH}$.

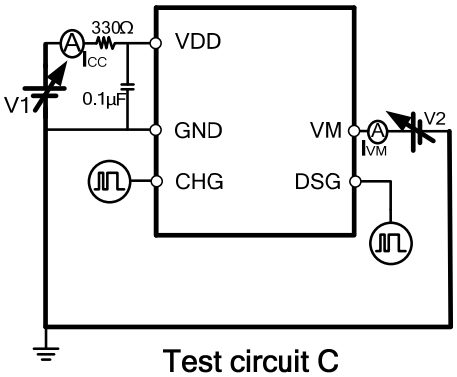
***Note7：*** ***When testing7-3($V_{DOC1}$),7-4($V_{SC}$),7-5($V_{DOCR}$),7-20($t_{DOC1}$),7-21($t_{SC}$),the VDD-1 will be adjusted only in 7-5,so we should add another 3.4V to VDD-1,in the other items,the VDD-1,PMOS and 10KΩ resistor could be removed for convenience.***



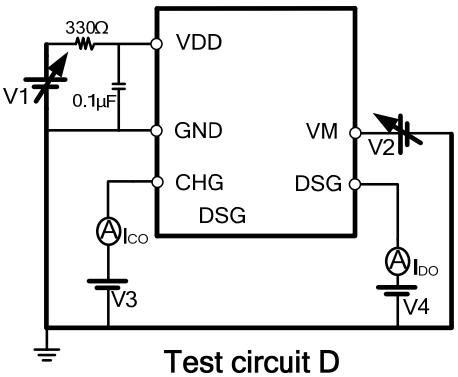

Test circuit A



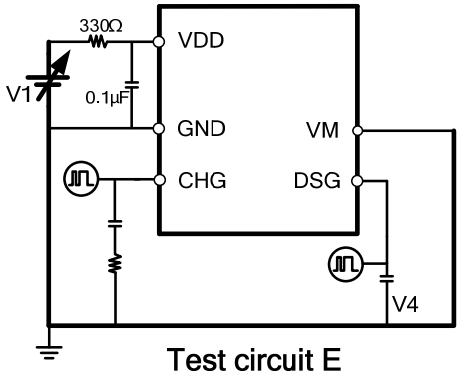

Test circuit B



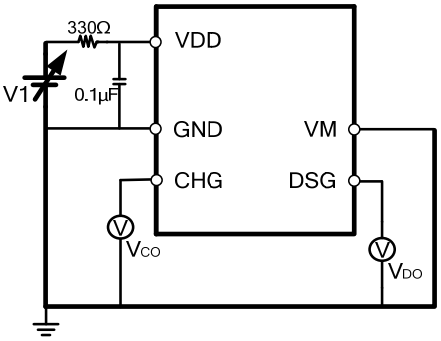

Test circuit C




Test circuit D




Test circuit E




Test circuit F

## 8 Typical application schematic

### 8.1 Application schematic of SH366303

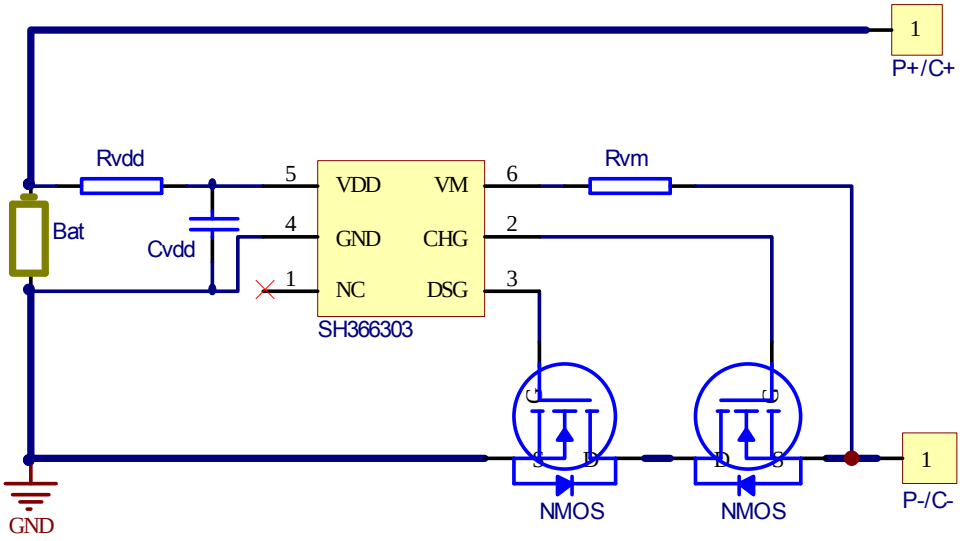


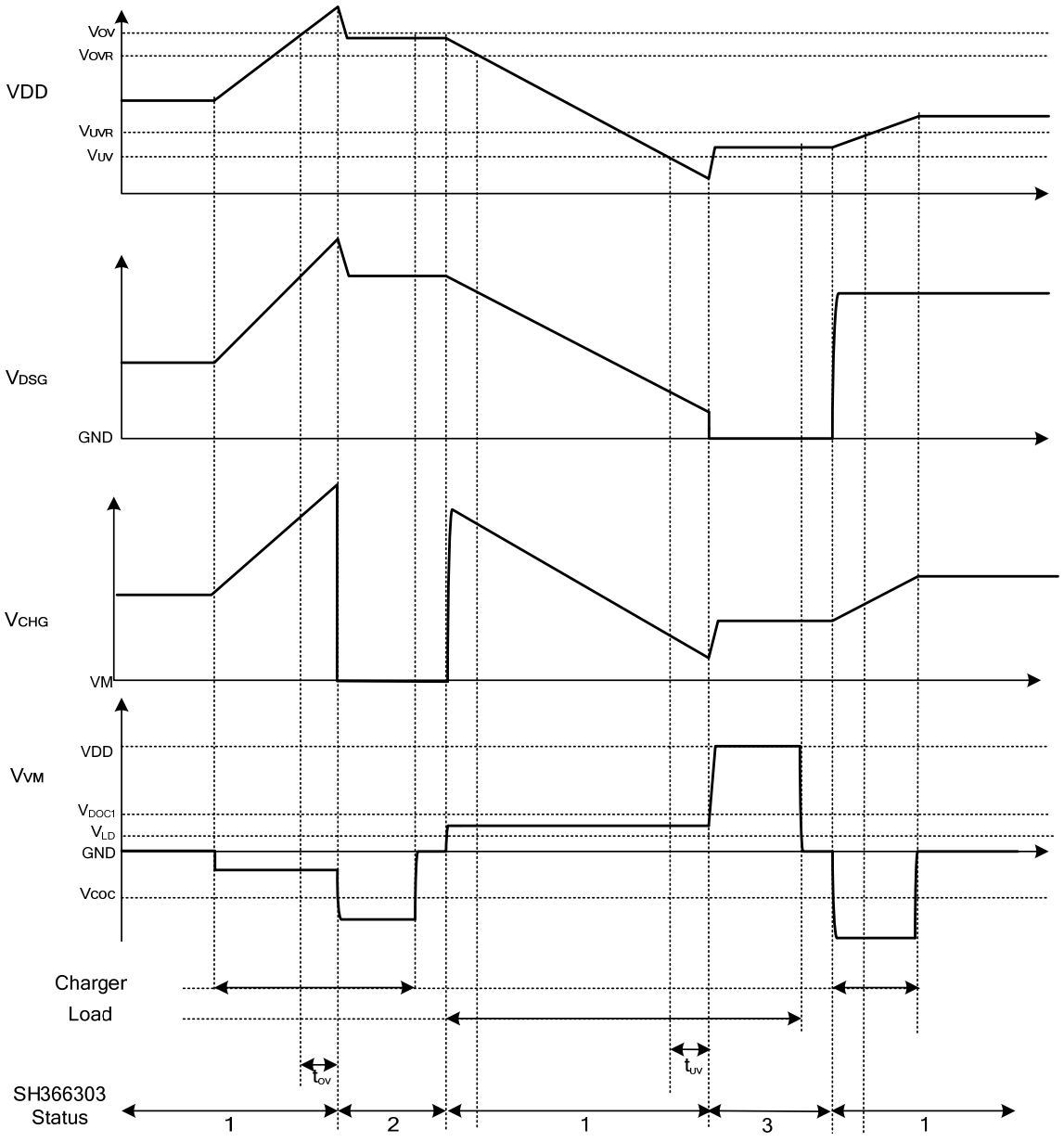

Fig 8. Application schematic of SH366303

### 8.2 External Components

| | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | $R_{vdd}$ | 100 | 330 | 1000 | Ω |
| 2 | $C_{vdd}$ | 0.068 | 0.1 | 1 | μF |
| 3 | $R_{vm}$ | 100 | 470 | 1000 | Ω |

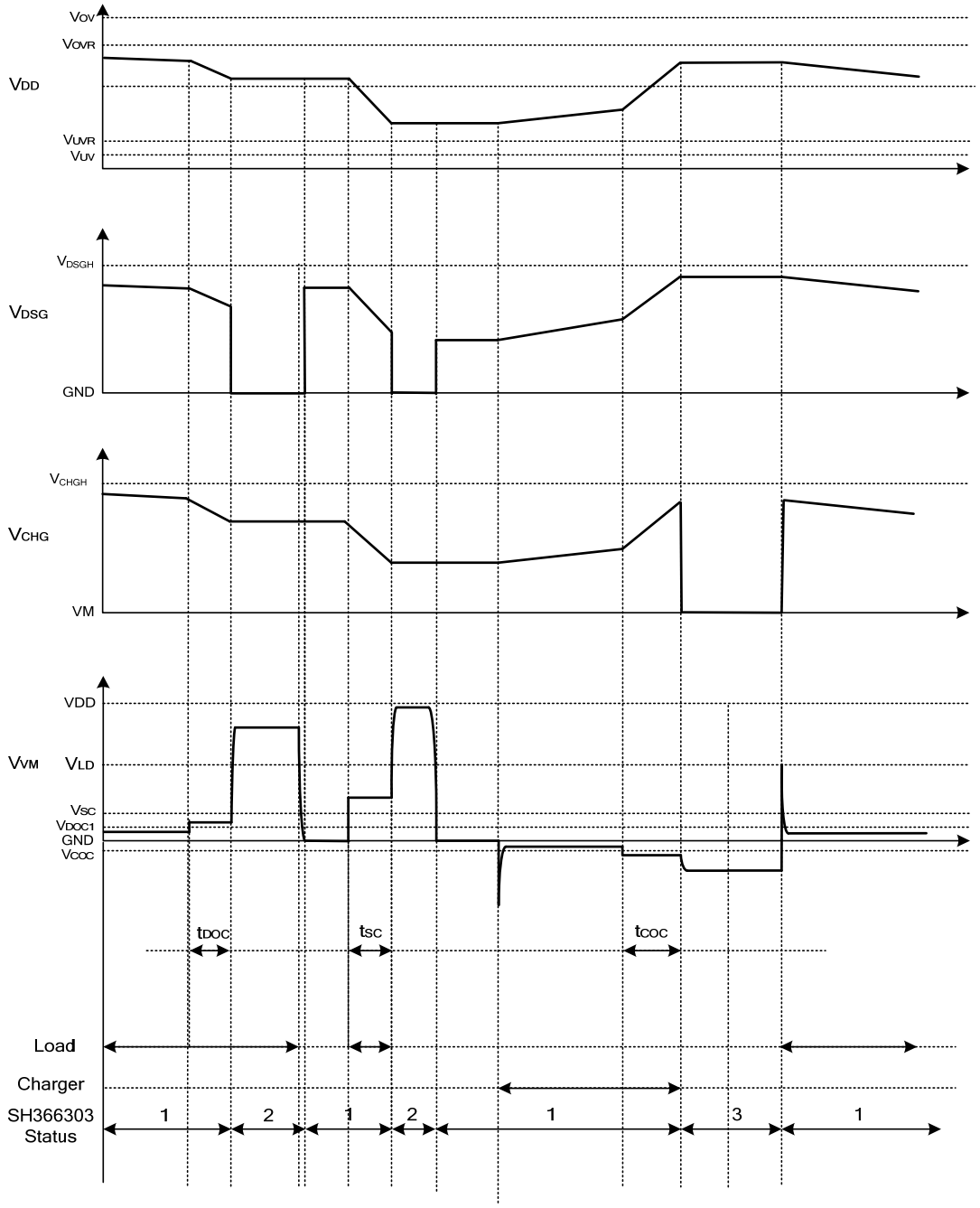
## 9 Timing Chart

### 9.1 Over-voltage and Under-voltage Chart




Status:
1.Normal status;
2.Over-charged status;
3.Over-discharged status;
tov:delay time of over-charged detection;
tuv:delay time of over-discharged detection;

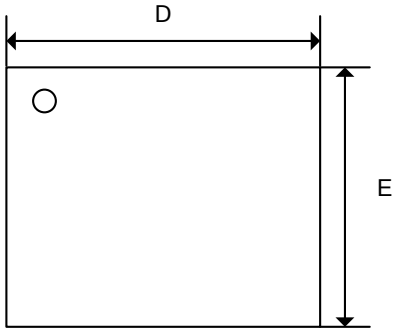
### 9.2 Over-current Operation Chart



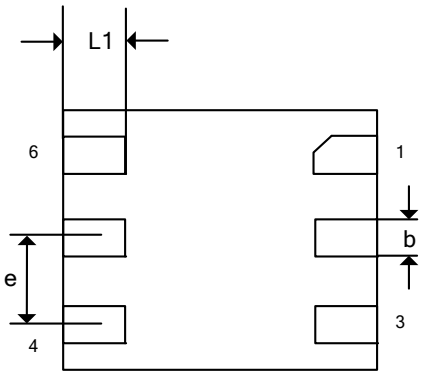

Status:
1.Normal status;
2. Discharging over-current status;
3.Charging over-current status;
$t_{DOC}$/$t_{COC}$:Delay time of discharging/charging over-current detection ;
$t_{SC}$:delay time of short-circuit detection;

## 10 Package dimensions

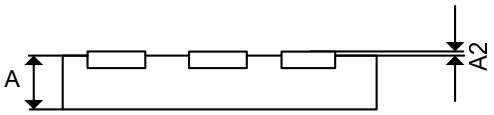
**DFN 6L (1.57 X 1.9) (P0.50 T 0.55) Outline Dimensions** **unit: mm**




Top View



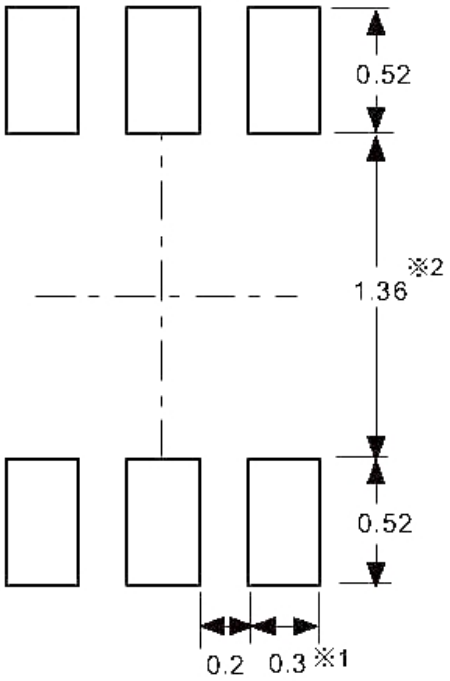

Bottom View




Side View

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | MIN | NOR | MAX |
| A | 0.5 | 0.55 | 0.6 |
| A2 | 0 | 0.025 | 0.05 |
| D | 1.8 | 1.9 | 2.0 |
| E | 1.47 | 1.57 | 1.67 |
| b | 0.17 | 0.22 | 0.27 |
| e | 0.5TYP | | |
| L1 | 0.25 | 0.30 | 0.35 |

Addition: the following dimension is the bonding pad of SH366303.



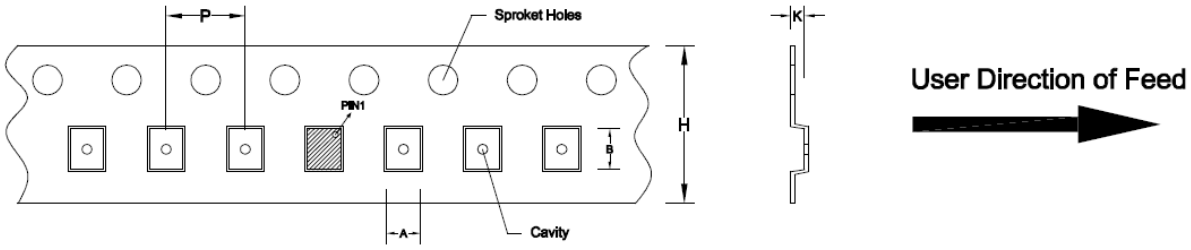

※Pay attention to the bonding pad width (0.25mm min./0.30 mm typ.)
※Don't widen the land pattern to the center of the package (1.30mm~1.40mm)

Caution: 1.Don't do silkscreen printing and solder printing under the mold resin of the package .
2.The thickness of the solder resist on the wire pattern under the package should be 0.03mm or less from the bonding pad surface .
3.Match the mask aperture size and aperture position with the bonding pad pattern .

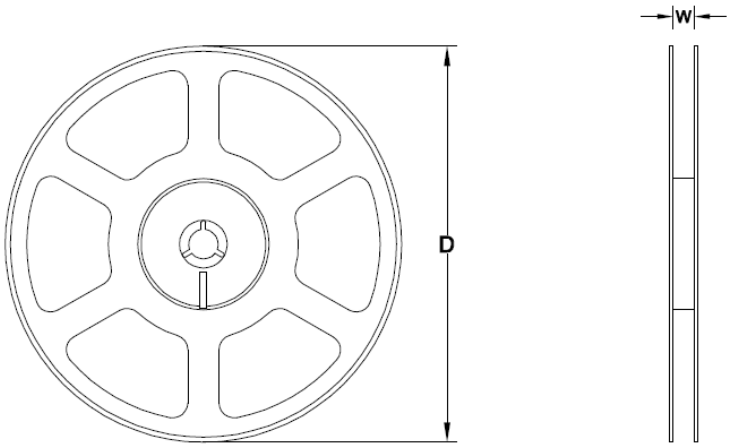
## 11 Carrier Tape and Reel Information

**DFN6L（1.57*1.9）** unit：mm

### Carrier Tape Dimensions



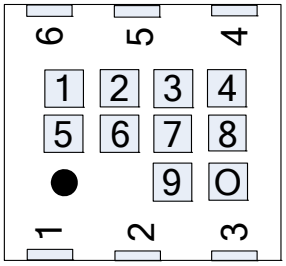

### Reel Dimensions




*All dimensions are **nominal**

| | | |
|---|---|---|
| A | 1.71 | Dimension designed to accommodate the component width |
| B | 2.08 | Dimension designed to accommodate the component length |
| K | 0.71 | Dimension designed to accommodate the component thickness |
| H | 8 | Overall width of the carrier tape |
| P | 4 | Pitch between successive cavity centers |
| W | 8.4 | Reel width |
| D | 178 | Reel diameter |

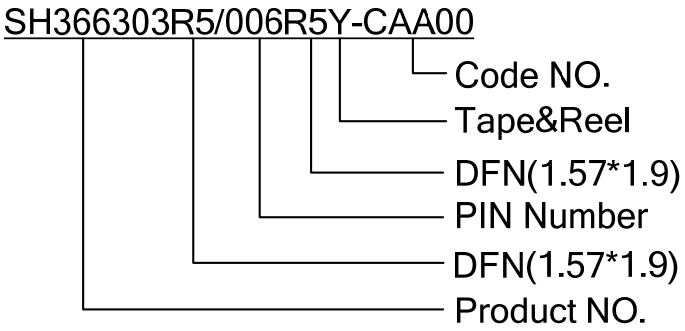
## 12 Mark Specification




Top view

①~④：Product abbreviations(5CAA);
⑤~⑧：Lot Number;
Last row: Year & month

## 13 Product Name Structure




## 14 Modification record

| Modification record of SH366303（CAA） | | |
|---|---|---|
| **Detailed description** | **Located pages** | **Date** |
| Original version V0.0 | - | 2019/12/25 |
| Add the bonding pad dimension and remove the parameter $I_{UV}$ | P6/8/10、P20 | 2020/07/08 |
| Add the specific description about test circuit | P11/12/13 | 2020/07/16 |
| Change the upper limitation of $V_{0INH}$ | P6/8/10 | 2020/07/22 |
| Add the specific description about discharging over-current release | P13 | 2020/08/05 |
| Change the upper and lower limit of $R_{VMS}$ in the sheet | P6/8/10 | 2020/09/14 |
| Change the typical value of $V_{0INH}$ in the sheet | P6/8/10 | 2020/10/30 |
| Change the test condition when measuring current consumption in over-discharged status | P16 | 2020/11/04 |
| Add the typical,Max and Min value in the sheet | P5~P10 | 2020/11/20 |
| Revise the test description and test circuit diagram | P15/16/17/18 | 2020/12/02 |
| Revise the package dimensions | P22 | 2020/12/09 |

**Link to the above:**

| | | |
|---|---|---|
| Convert the parameters which reflect drive capability from $I_{DH}$,$I_{CH}$,$I_{DL}$,$I_{CL}$ to $R_{DH}$,$R_{CH}$, $R_{DL}$,$R_{CL}$,meanwhile,revise the related test description. | P6/8/10,P16 | 2020/12/23 |
| Convert $R_{DL}$ in the sheet from 0.5kΩ to 3.1kΩ@Typical | P6/8/10 | 2021/01/25 |
| | | |